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***Abstract*—In this paper, we investigate a test strategy for characterization of clock error statistics between two clock domains in high-speed clocking systems (gigahertz and more). The method allows an indirect measurement (not based on time interval measurement) of clock error distribution by observing the integrity of a periodic sequence transmitted between two clocking domains. The method is compatible with fully on-chip implementation, and the readout of result to off-chip signals is cadenced at low rate. The strategy aims at picoseconds resolution without complex calibration. The idea was first validated by a discrete prototype at downscaled frequencies, and then a high frequency on-chip prototype was designed using 65 nm CMOS technology. Simulation results predict a measurement precision of less than $\pm$2.5 ps. The article presents the theory, exposes the hardware implementation, and reports the experimental validation and simulation results of two prototypes.**

***Keywords*-clock domains, static and dynamic error, controlled delay, metastability.**

I. Introduction

In modern large-scale integrated circuit, a global clock distribution system is used to synchronize communications between various points in the system [1] [2]. A synchronous communication requires the clocks at the transmitter and receiver sides to be perfectly synchronized. In practice, a perfect synchronization is impossible: the must-be-simultaneous clock events are separated by time intervals called "clock error". The awareness of the maximal clock error is necessary for establishment of timing budget for communication and data processing.

Clock uncertainty or phase error (Δt_i) between two clocks clk1 and clk2 with the same average period T is defined as clk2 i^{th} edge arriving time t_i^2 minus clk1 i^{th} edge arriving time t_i^1 (Fig. 1). Here i is the index of clock cycle. Due to periodic property of clock signals, Δt_i can be expressed as [3]

$$\Delta t_i = (T/2 + t_i^2 - t_i^1) \bmod T - T/2. \quad (1)$$

where mod represents modulo operation. In this study, phase error between clocks is supposed to be much smaller than the average (nominal) clock period, and no dependency exists between Δt_i. These are reasonable assumptions in on-chip clocking context.

$\{\Delta t_i\}_{i\in\mathbb{N}}$ is a discrete time random process characterized by the time average $S_{in} = \overline{\Delta t}$ called *skew* and the dynamic component of the phase error $\{\Delta t_i - S_{in}\}_{i\in\mathbb{N}}$. This process

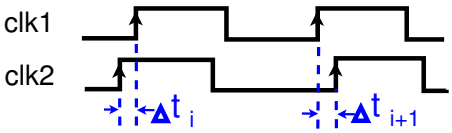


Fig. 1: Definition of the clock error Δt_i

is usually considered as ergodic. The values of a realization of the process $\{\Delta t_i\}_{i\in\mathbb{N}}$ are characterized by a distribution function, which is also a probability density function (PDF) since the process is ergodic. In practice, a probability density function of a clock error is a function defined on a limited domain with maximal and minimal non-zero values B and C (for example, a truncated Gaussian distribution as in Fig. 2).

The measurement of clock error can be required in many cases. This work is motivated by the need for characterizing clocks generated by an alternative method using a network of coupled oscillators [4]. The typical clock errors for gigahertz clocks are of tens of picoseconds or less. An off-chip measurement requires the transmission of clock signals off the chip, thus introducing additional delays whose values are difficult to control [5] [6]. The sampling rate and the vertical gain of available measurement tools are also major issues.

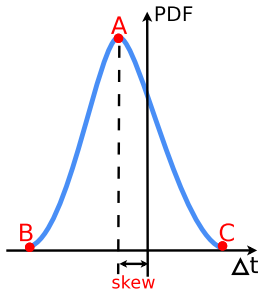


Fig. 2: Gaussian distribution of clock phase error

On-chip solutions are usually based on time measurement techniques using a cascaded delay chain [7]. However, the minimum delay of a buffer is of the same order as the clock error to be measured. Improvement is achieved by using a Vernier delay line [8] [9] [10]. These architectures use two parallel buffer chains with different delays: the time difference between the buffer delays defines the measurement resolution.

However, when the absolute value of the clock error should be known, the on-chip measurement needs a complex calibration. Several works aiming a direct measurement of the clock error use a delay chain based time-to-digital converter with a large number of stages (e.g., 129 in [7]). The outputs of the TDC stages are then processed by digital circuits at high rate. Although such a method provides precise value of timing error in each period, it is area and energy expensive, since in most cases only the statistics about the clock error are required (the mean, the minimum and the maximum values).

The technique proposed by this paper is based on an integrity check of a periodic sequence transmitted from one clock domain to the other. If there is a clock error, the received sequence contains errors. The error rate is related to both static and dynamic errors between two clock domains. To characterize the process $\{\Delta t_i\}_{i\in\mathbb{N}}$, an externally controlled on-chip delay element is inserted in the test sequence data path. By varying the delay value, the error rate is modulated, and then the intrinsic clock error characteristics of the process $\{\Delta t_i\}_{i\in\mathbb{N}}$ can be abstracted by a simple processing unit. Only one bit is processed at each clock cycle, different from existing methods based on direct time interval quantification (e.g., 129 bits are processed in architecture described in [7]).

The measurement resolution is defined by precision of the delay control. An on-chip delay with a high precision (few ps) can be achieved by techniques described in section IV.

The paper is organized as follows. Section II explains measurement principle and proposed circuit. In section III, the discrete device prototype and measurement results are presented. Post-layout simulation results of ASIC prototype are exhibited in section IV.

II. Test Methodology

The proposed test method is based on the architecture presented in Fig. 3, which detects the variation of the sign of clock error Δt. It is done in the following way. The test pattern generator issues a periodic sequence "...010101..." which is synchronized with clk1. This pattern is transmitted to the clk2 domain, and a processing unit block checks its integrity. The received pattern is considered correct if and only if it is the same as the sent pattern. The circuit cannot detect the delay between two patterns since they are not in the same clock domain. Hence, if Δt sequence is constant (only a static error is present), the transmission is always correct (Fig. 4(a)). This circuit cannot detect a pure static error (skew) between clocks.

However, if the clock error has a dynamic component – which is a common case – the clock error may change its sign. In this case, the sequence received by the processing unit contains two successive 0 or 1 (Fig. 4(b)): the integrity of the sequence is violated and can be detected by the processing unit. After that, digital circuits can easily estimate the error rate ER. The error rate obtained from such a measurement is related to both the static and dynamic component of the clock error. For example, if the skew is greater than the amplitude of the dynamic component, the sign never changes, and the detected error rate is zero. If there is no skew, the sign change happens on average once over two clock events, and the measured error rate is 1/2.

Now we insert a controlled delay Δ in the transmission path(Fig. 3). This delay is equivalent to an additional skew between the clocks. By varying the delay Δ, we change the effective skew, hence, the measured error rate (ER), which is now a function of Δ. The next section shows the analysis providing the relation between the measured function $\mathrm{ER}(\Delta)$ and the unknown PDF of the clock error.

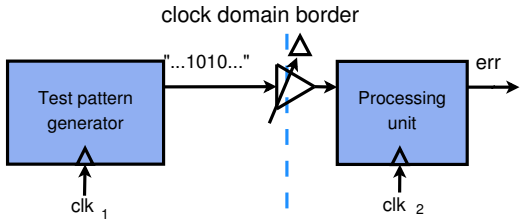


Fig. 3: Basic architecture of measurement circuit

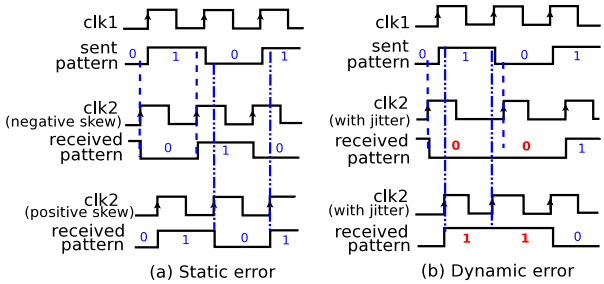


Fig. 4: Received data integrity

A. Measurement theory

The introduction of the delay Δ (Fig. 3) modifies the skew between the clocks, and hence the effective PDF of the clock error distribution, by mapping $\Delta t \rightarrow \Delta t + \Delta$ (Fig. 5(b)). According to the definition of phase error (formula (1)), a positive delay Δ has a negative effect on the effective phase error, thus the effective skew is $S_{in} - \Delta$. We can find a mathematical relation between the error rate ER and the original PDF of clock error by observing two neighboring clock cycles.

The error rate represents the probability of the sign change of the effective (modified by the delay) clock error. Considering that there is no dependency between Δt_i, we have :

$$\begin{aligned} \mathrm{ER} &= P(\Delta t_i > 0)P(\Delta t_{i-1} < 0) \\ &\quad + P(\Delta t_i < 0)P(\Delta t_{i-1} > 0) \\ &= 2P(\Delta t_i < 0)P(\Delta t_{i-1} > 0) \\ &= 2P(\Delta t_i < 0)(1 - P(\Delta t_i < 0)) \\ &= 2a(1-a), \end{aligned} \tag{2}$$

where $a(\Delta) = P(\Delta t_i < 0)$ is the probability that the i^{th} cycle phase error is negative (Fig. 5(a)). $a(\Delta)$ is given by:

$$\begin{aligned} a(\Delta) &= P(\Delta t_i < 0) \\ &= \int_{-\infty}^{0} \mathrm{PDF}(z+\Delta)dz = \int_{-\infty}^{\Delta} \mathrm{PDF}(y)dy. \end{aligned} \tag{3}$$

When Δ is equal to the intrinsic skew S_{in}, on average, clock errors are positive in 50% of clock cycles and negative in the other 50% cycles. In this case the measured error rate is equal to $1/2$ and is maximal. This allows a measurement of the intrinsic skew. To find the original PDF, the expression (3) is derived:

$$\mathrm{PDF}(\Delta) = \frac{\partial a}{\partial \Delta}. \tag{4}$$

According to the definition of $a(\Delta)$, a is greater than 1/2 when the effective skew $S_{in} - \Delta$ is positive, otherwise, a is less than 1/2. Hence, from (2), a can be expressed as:

$$a = \begin{cases} \dfrac{1+\sqrt{1-2\mathrm{ER}}}{2} & \Delta \geq S_{in} \\ \dfrac{1-\sqrt{1-2\mathrm{ER}}}{2} & \Delta < S_{in} \end{cases} \tag{5}$$

By differentiating, (5) turns into the following equation:

$$\frac{\partial a}{\partial \Delta} = \frac{1}{\sqrt{1-2\mathrm{ER}}} \frac{\partial \mathrm{ER}}{\partial \Delta} \mathrm{sign}(S_{in} - \Delta). \tag{6}$$

where $\mathrm{sign(x)} = \begin{cases} 1 & x \geq 0 \\ -1 & x < 0 \end{cases}$

From (4) and (6), we obtain:

$$\mathrm{PDF}(\Delta) = \frac{1}{\sqrt{1-2\mathrm{ER}}} \frac{\partial \mathrm{ER}}{\partial \Delta} \mathrm{sign}(S_{in} - \Delta). \tag{7}$$

The $\mathrm{PDF}(\Delta)$ calculated by the formula (7) is non-zero only when the variation of function $\mathrm{ER}(\Delta)$ doesn't equal zero. Hence, the maximal and minimal dynamic error values (points B and C in Fig. 5(a)) can easily be calculated. The largest and the smallest Δ values at which $\mathrm{PDF}(\Delta)$ is non-zero are given by the limit of the Δ range at which $\mathrm{ER}(\Delta)$ is non-zero (points B and C in Fig. 5(d)). Indeed, the delay $\Delta = \Delta t_B$ or $\Delta = \Delta t_C$ shifts the original PDF rightward/leftward until $a = 0$ or $a = 1$. Hence, Δ_B and Δ_C correspond respectively to Δtd values at points B and C of original PDF (Fig. 5(a)), which are the min/max clock error values.

However, to abstract the full original PDF of clock error, Δ must be positive or negative. A real delay is always positive. However, a negative delay can be imitated by two methods. The first way is to use a single variable delay whose value could be close to the clock period. The relation between Δ and the implemented physical delay Δtd can be expressed by the following equation:

$$\Delta = (T/2 + \Delta td) \bmod T - T/2. \tag{8}$$

In this case, the ER distribution with respect to the real delay value is illustrated in Fig. 6, where delay values at points A, B, and C correspond to skew and min/max errors.

The second way to have a negative delay is to use a differential delay pair – one delay for each clock domain. Therefore, the real delay introduced between two clocks is the difference value between two delays. If the range of a single delay is [a, b], that of a differential delay using two identical delays is [-(b-a), b-a].

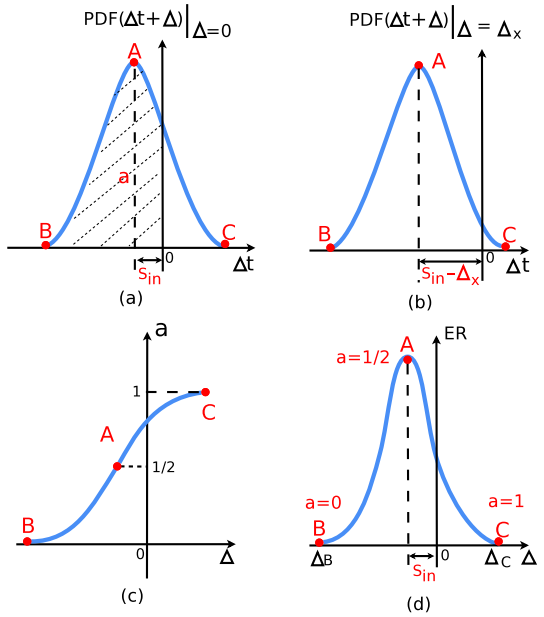


Fig. 5: (a) Original PDF of clock uncertainty; (b) PDF with a shift $\Delta = \Delta_x$; (c) a vs. Δ; (d) ER vs. Δ

We have studied the two techniques in our work: the former technique has been implemented in a low frequency discrete circuit prototype (cf. section III); the latter has been implemented in a high frequency ASIC prototype (cf. section IV).

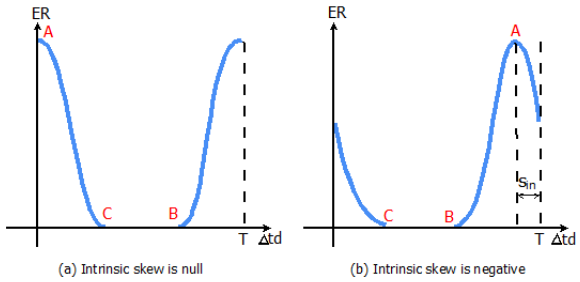


Fig. 6: ER distribution with respect to single positive delay

B. Architecture of measurement circuit

The measurement circuit is implemented as shown in Fig. 7.

A binary sequence "...1010..." is generated on-chip in clk1 domain by a D flip-flop synchronized with the clock clk1 (Fig. 7). The binary sequence is sent to the clk2 clock domain after a controllable delay (Δ), which allows varying the effective static error between two clocks manually.

The data sequence is sampled in the clk2 domain. To avoid metastability in flip-flops [11], a 4-stage shift register cadenced by clk_2 and $\overline{clk_2}$ samples the input signal (D2) of the clk2 domain. A 2-input NXOR gate detects transmission errors by comparing R3 and R5 outputs; each detection event is then counted by the n-bit counter C1 cadenced by clk2. The role of the counter C2 is to generate an event every $2^n - 1$ clk2 cycles:

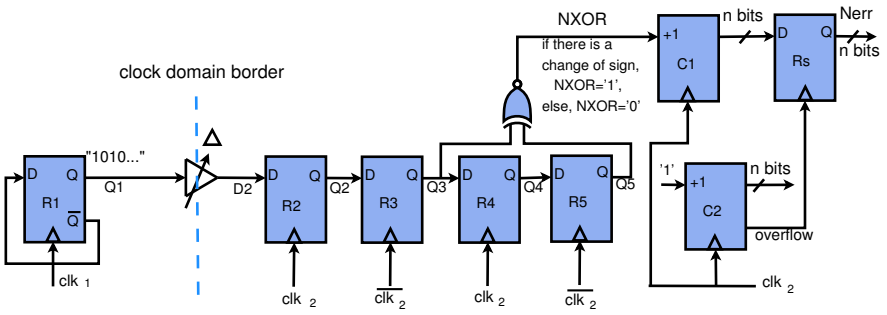


Fig. 7: Architecture of test circuit

this provides a time interval during which C1 counts the errors. The value of C1 is written into the output register Rs when C2 overflows. Metastability is avoid because the NXOR updates at the falling edge of clk_2 while the counters work at the clk_2 rising edge. The register Rs stores the signal Nerr value. It represents the number of errors during $2^n - 1$ clk2 cycles and can easily be transmitted off-chip, because the readout is at a frequency 2^n lower than the clock frequency.

III. Low frequency discrete circuit prototype

A low frequency prototype using discrete devices is implemented to evaluate the proposed test method. Two 8-bit counters (C1 and C2 in Fig. 7) are implemented for sign changes rate calculation. A 8-bit register (Rs) samples the counter result every 255 clock cycles. Negative delays are implemented with the first technique described in section II.A.

clk1, a 500 KHz signal with a 50% duty cycle, is generated by a function generator. The clock clk2 with dynamic error and skew is generated from clk1 by the circuit in Fig. 8. RC delay provides a positive delay (a negative skew is obtained by generating clk2 from clk1). A clock edge uncertainty with max/min value of ± 100 ns is achieved by adding a noise signal over the power supply of inverter. To eliminate glitches, a Schmitt trigger is used at the output.

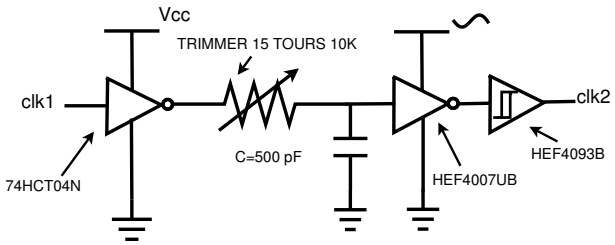


Fig. 8: Generation of clk2 with static and dynamic errors

The controllable variable delay Δtd is implemented as a 4-stage delay chain shown in Fig. 9, in which the resistor is a trimmer. Four delay stages could generate a large delay with a value comparable to the period of the sequence Q1. To acquire the function $ER(\Delta td)$, the delay Δtd varies from 0 to 2 μs and the output ER value is observed.

We have performed two tests to evaluate the prototype. In the first test, only pure dynamic errors without skew ([-100 ns, 100 ns]) are added. The measured error range is [-120 ns, 130 ns] as illustrated in Fig. 10a. In the second test, a negative skew of 40 ns exists along with ± 100 ns dynamic errors. Test result shown in Fig. 10b (mean value -50 ns, range [-150 ns, 80 ns]) is in good agreement with the values we measured directly (mean value -40 ns, range [-140 ns, 60 ns]). The obtained plots (Fig. 10) are qualitatively similar to those predicted by theory (Fig. 6).

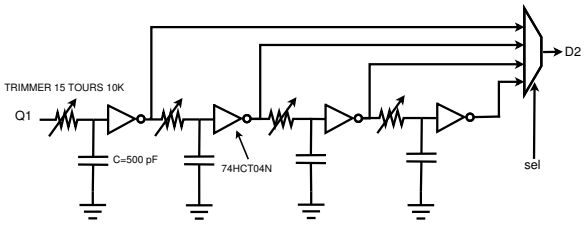
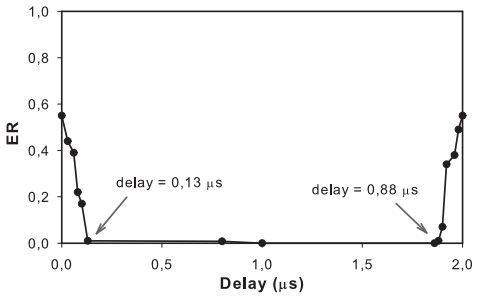
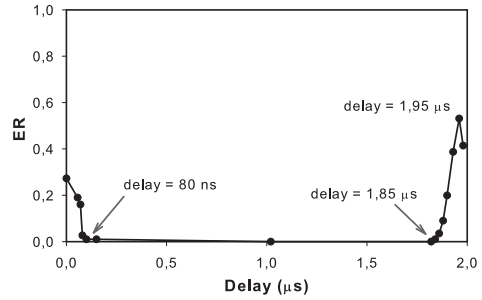


Fig. 9: Variable delay circuit in discrete circuit prototype



(a) without skew



(b) with a skew of -40 ns

Fig. 10: Test of prototype with or without skew

IV. High frequency on-chip prototype

The main drawback of the discrete prototype comparing with its on-chip implementation consists in the implementation of the delay Δ: First, an approximation of a pure delay by RC networks is only efficient for delays largely inferior to characteristic time of the signals. However, the method needs pure delays of the same order as the signal period; Second, small values of Δ are difficult to implement, because of the threshold imposed by intrinsic technology delays. To overcome these difficulties, Δ is defined as differential delay. The new topology of the on-chip measurement system is shown in Fig. 11. One variable delay $\Delta td1$ is used in the test pattern path, the other delay $\Delta td2$ is applied to the clock $clk2$. As explained in section III.A, the effective delay value is $\Delta = \Delta td1 - \Delta td2$, which can be a very precise value (positive or negative) close to zero. Moreover, the delay range is doubled. No calibration is needed because we can always know the current delay values by observing $\Delta td_{measurement}$. Implementation details and characteristics of proposed variable delay are presented in the next subsection.

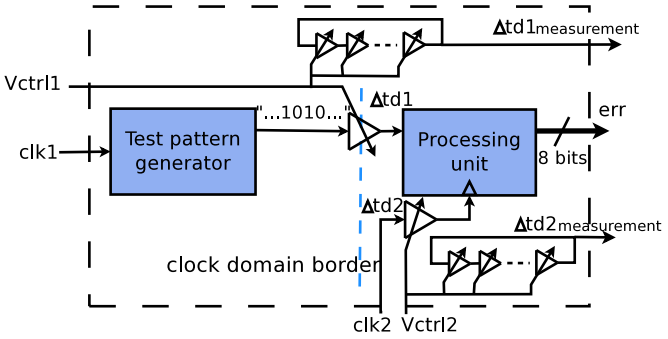


Fig. 11: ASIC prototype architecture

A. Voltage-controlled delay

The voltage controlled delay element is based on the topology in Fig. 12. It is composed of two CMOS inverters. The propagation time of a current starved inverter (M4-M5) is controlled by the charging and discharging currents through the input voltage V_{ctrl}. The second inverter (M8-M9) improves the rising and falling edges of output signal.

In this prototype, to have a large delay range, two delay elements in Fig. 12 are cascaded. To be aware of the delay during measurement, a replica of variable delay is repeated and set as a ring oscillator. Since the exact delay value is known during the test, a complex calibration is no more necessary.

Fig. 13 shows the delay-voltage relations at different input signal frequency conditions and the delay measured by ring oscillator. From Fig. 13, we can observe that if the control voltage is greater than 0.85 V, the delay value used for manipulation matches the value measured by oscillator with a difference of less than 2 ps. The delay range is [333.89 ps, 435.97 ps] for one delay, hence for the differential delay the range is [-102 ps, 102 ps]. The latter range is large enough comparing with typical phase errors between synchronized

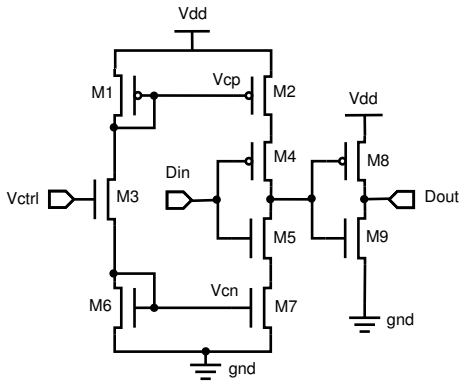


Fig. 12: Voltage-controlled delay element [12]

high frequency on-chip clocks. The resolution of the differential delay control is about 2 ps/5 mV at high control voltage and 5 ps/5 mV at low control voltage. A step of 5 mV with a precision of less than 0.05% can be achieved by a modern voltage supply device (ex. Agilent 6625A Power Supply); therefore we can have a precision of ± 1 ps for small clock error measurements and ± 2.5 ps for large error.

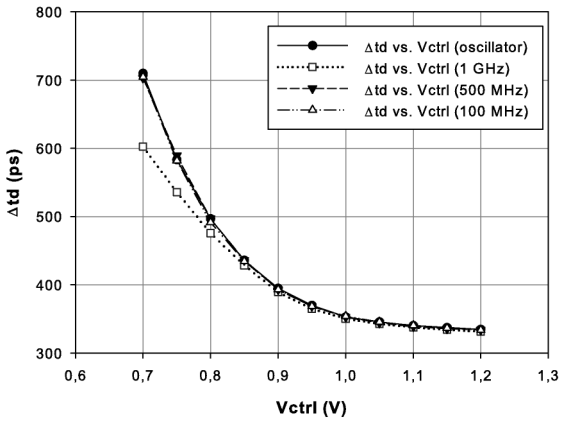


Fig. 13: Variable delay in function of control voltage

B. Simulation results

To evaluate the proposed circuit, we performed a post-layout simulation. In the testbench, normally distributed phase errors are added between two 1 GHz clock signals. The mean value (skew) is -20 ps and max/min error values are 19.6 ps/-53.4 ps. The histogram of the generated clock error distribution during 1020 cycles is displayed in Fig. 14.

The error rate (ER) is calculated by dividing the total number of errors during 4 cycles of test (255 periods each cycle) by 1020. The measured $\mathrm{ER}(\Delta)$ curve is drawn in Fig. 15. Table. I records detailed results of each step. The measurement allows a localization of the minimum error in the interval of [-54.63 ps, -49.05 ps], whereas the real minimum error value is -53.4 ps, a precision of [-1.23 ps, 4.35 ps] is

TABLE I: Post-layout simulation results

Vctrl1 (V)	Vctrl2 (V)	$\Delta td1$ (ps)	$\Delta td2$ (ps)	Δ (ps) $(\Delta td1 - \Delta td2)$	err (255 periods each cycle)					Error rate
					1^{st} cycle	2^{nd} cycle	3^{rd} cycle	4^{th} cycle	total	
0.945	0.86	370.06	424.69	-54.63	0	0	0	0	0	0
0.955	0.87	366.31	415.36	-49.05	10	2	2	8	22	0.0217
0.955	0.875	366.31	410.96	-44.65	14	4	4	12	34	0.0335
0.955	0.88	366.31	406.86	-40.55	30	14	10	22	76	0.0748
0.95	0.885	368.13	403.11	-34.98	56	34	37	44	171	0.1683
0.95	0.89	368.13	399.67	-31.54	70	58	47	58	233	0.2293
0.95	0.9	368.13	393.13	-25	117	108	101	121	447	0.4400
0.95	0.91	368.13	387.12	-18.99	123	126	127	122	498	0.4902
0.94	0.91	372.11	387.12	-15.01	111	110	106	104	431	0.4242
0.93	0.91	376.61	387.12	-10.51	71	82	88	86	327	0.3219
0.92	0.91	381.67	387.12	-5.45	53	54	58	58	223	0.2195
0.91	0.91	387.12	387.12	0	25	30	32	18	105	0.1033
0.91	0.92	387.12	381.67	5.45	5	6	8	6	25	0.0246
0.91	0.93	387.12	376.61	10.51	0	0	2	4	6	0.0059
0.91	0.94	387.12	372.11	15.01	0	0	2	2	4	0.0039
0.91	0.955	387.12	363.31	20.81	0	0	0	0	0	0

achieved. In the same way, the maximum error is between 15.01 ps and 20.81 ps, which has a difference lying in the range [-4.59 ps, 1.21 ps] with respect to the real value 19.6 ps. If we define the median value of the range as an estimation of real value, we find that the estimation error is within ± 2 ps. The measured skew is -18.99 ps, which is 1.01 ps larger than the real value. The measurement results demonstrates a good precision in accordance with the theory.

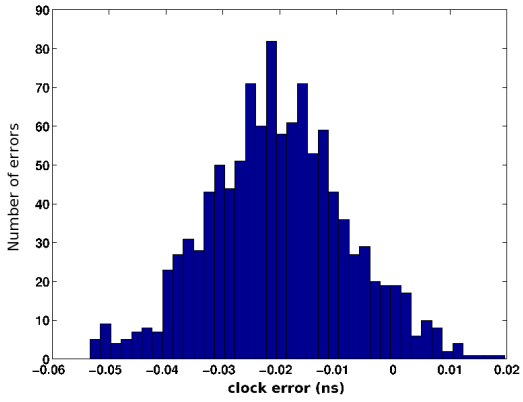


Fig. 14: Histogram of clock errors between clk1 and clk2

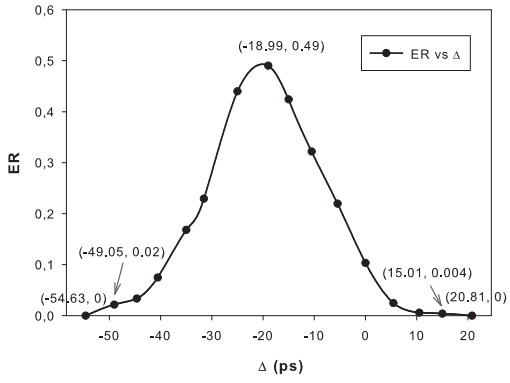


Fig. 15: ASIC prototype error rate

V. Conclusion

A simple test circuit is proposed to evaluate the clock error statistics between two clock signals in chip. It provides an easy and straightforward way to measure static error (skew) and minimum/maximum dynamic error values. Not based on a direct time interval measurement, this on-chip test method reduces cost and difficulty of high frequency clock distribution quality test. The method was validated experimentally on a low-frequency discrete prototype, and a high-frequency integrated prototype was designed in 65nm CMOS technology and validated by simulation.

Acknowledgment

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