Automated triangular wave generator design with process corners compensation

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***Abstract*—In this paper, a systematic design methodology is proposed to design a triangular wave generator circuit. Using this methodology, various oscillation frequencies can be obtained in a shorter design time. Furthermore, the variations in the oscillation frequency are controlled across all process corners. The proposed methodology employs a transistor sizing and biasing CAD tool called CHAMS, in which the sizes and biases of each transistor are performed to meet the required DC operating points. Across all process corners, the error in the oscillation frequency can be controlled by changing the trimming current. Simulations across nine corners are done to estimate the error in frequency. The condition to pass the design is to guarantee that for each process corner, at least one of the trimming combination sets the oscillation frequency within the specified limits. The methodology is applied for different arbitrary values of frequencies 1 MHz, 2 MHz, and 4 MHz with a maximum error of $\pm 3\%$.**

I. Introduction

Triangular wave generators are widely used in many applications such as instruments, measurements, switching power conversion control circuits. In switching power converters, such as DC-DC converters, triangular wave generator is used to provide the reference switching frequency of the system. Variations in the switching frequency affect the converter output voltage ripples. Hence, the error in the switching frequency has to be minimized [1], [2].

As the triangular wave generators are widely used, the availability of efficient systematic design procedure to design such circuits would be useful and shorten the design time.

In this work, a structured design methodology is proposed for a triangular wave generator. The methodology utilizes a structured computer-aided-design (CAD) tool developed in LIP6-UPMC called CHAMS. Using this methodology, the triangular wave generator circuit can be sized to obtain different oscillation frequencies with less design time. Moreover, a current trimming circuit is sized to sustain an oscillation frequency within certain error limits across all the process corners. In the design methodology certain circuit specifications - such as, propagation delay of comparator - are set. Then, the sizing and biasing of the all components can be provided automatically.

The paper is organized as follows. Section II describes the triangular wave generator architecture, including the comparator and trimming circuits. An overview of CHAMS concept of operation is discussed in Section III and illustrated by the comparator circuit design of the wave generator. Section IV shows the design flow for the trimming circuit. Simulation results are reported in Section V. In Section VI, conclusions are drawn.

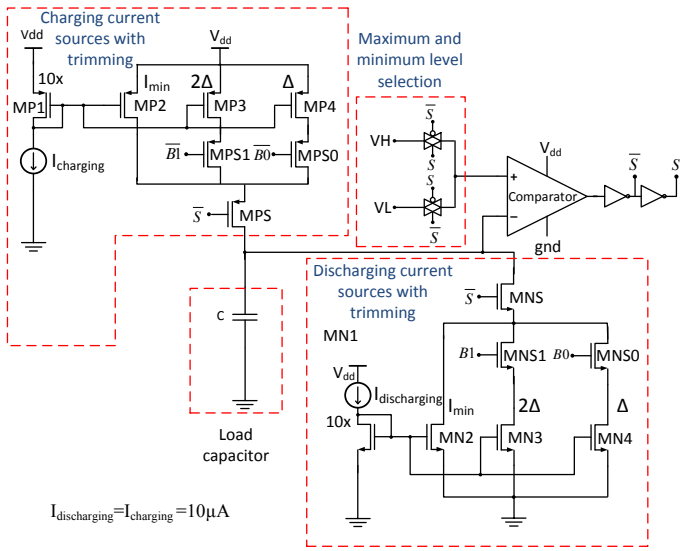

Fig. 1: Triangular wave circuit schematic

II. Triangular wave generator circuit

The triangular wave generator circuit is illustrated in Figure 1. A capacitor is charged and discharged via constant current sources. The voltage across the capacitor is compared to reference voltages V_L and V_H, which represent the minimum and maximum voltage levels of the triangular wave signal.

The basic circuit operation can be divided in two cycles which are charging and discharging cycles. In the charging cycle, the PMOS switch (MPS) is turned on and the current source charges the capacitor. When the capacitor voltage exceeds V_H, the comparator signal ($\overline{S}$) switches off the PMOS switch (MPS) and turns on the NMOS switch (MNS) starting the discharging cycle. The resistances of the switches (MPS and MNS) should be minimized to reduce the variation of the transistor drain voltages in the current mirrors.

The triangular wave period can be calculated using equation 1:

$$\begin{aligned} T_{triangular} &= T_{charging} + T_{discharging} \\ &= \left(\frac{1}{I_{charging}} + \frac{1}{I_{discharging}}\right).C.(V_H - V_L) \end{aligned} \quad (1)$$

where C is the load capacitor, $I_{charging}$ and $I_{discharging}$ are the capacitor charging and discharging currents, respectively. $I_{charging}$ and $I_{discharging}$ have the same value in order to have a triangular wave with equal rising and falling times. The current trimming is used to compensate the variations in the frequency due to the process variations. The compensation is performed by controlling different current sources using input trimming bits (B0 and B1) to select different bias currents. The trimming bits (B0 and B1) are externally asserted to obtain the proper oscillation frequency. As two trimming bits are used, four current values can be generated. Across all process corners, the required oscillation frequency should be obtained using one of these four current values. The number of series switches is minimized in order to reduce the current discrepancies in the current mirror. The trimming circuit presented has a maximum of two series switches in each branch. With process corners variation, a current variation range is estimated. Minimum current (I_{min}) is to compensate for the worst power corners and maximum current (I_{max}) to compensate for the worst speed corners. Current mirrors are designed with minimum current (I_{min}) and two current sources of currents equal to Δ and 2Δ, where :

$$\Delta = (I_{max} - I_{min})/3. \tag{2}$$

The current values for the trimming circuit are defined as: $(I_{min}, I_{min} + \Delta, I_{min} + 2\Delta, I_{max})$. Currents I_{min} and I_{max} are varied to sustain the oscillation frequency with limited variations across all the process corners.
The comparator architecture is shown in figure 2. It comprises three stages of amplifiers. The first stage is a conventional differential pair amplifier. The second and third stages are common source amplifiers. The transistors MN7 and MN6 are used to clamp the output voltage of the second stage, hence, minimize the swing and speed up the comparator. The third stage gain is maximized to sense the small voltage swing at its input. An inverter is used to enhance the load driving capabilities. The comparator is designed to minimize the propagation delay in order to minimize the error in the amplitude of the triangular wave.

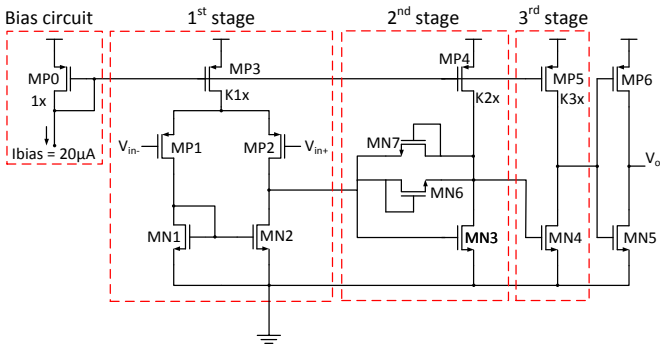

Fig. 2: Comparator circuit schematic

III. CHAMS: Hierarchical sizing and biasing methodology

CHAMS is a CAD platform that provides assistance to the analog designer for the design of analog firm intellectual properties (IP) [3]–[5], it is developed at LIP6 [6]–[8]. CHAMS allows to generate the analog IP sizing and biasing procedure. CHAMS has the following features:

- It is based on the C/C++ language.
- It implements a standard interface for the encapsulation of a spice-like electrical simulator.
- It has a fast *transistor* sizing and biasing tool based on MOS *operators*.
- It has a fast *circuit* sizing and biasing tool based on a *bipartite graph*.
- It injects sizing and biasing knowledge during an optimization phase.

Sizing and biasing operators aim at computing the sizes and biases of transistors. The operators are based on the numerical inversion of the transistor compact model (BSIM3v3 [9], BSIM4 [9], EKV [10], PSP [11]). Every transistor is defined by the following parameters: W (width), L (length), V_{GS} (gate-source voltage), V_{DS} (drain-source voltage), V_{BS} (bulk-source voltage), V_{EG} (overdrive gate voltage), I_D (drain current), $Temp$ (temperature). Each operator has a set of input parameters that are set by the designer and computes unknown widths and biases (see Table I, where $V_{EG} = V_{GS} - V_{TH}$ enables to use the $\frac{g_m}{I_d}$ method [12]). An operator computes either:

$$W = f_W(Temp, I_D, L, V_{GS}, V_{DS}, V_{BS}) \tag{3}$$

or :

$$V_{GS} = f_{V_{GS}}(Temp, I_D, W, L, V_{DS}, V_{BS}) \tag{4}$$

f_W and $f_{V_{GS}}$ are two inverse functions of the transistor compact model given in equation (5):

$$I_D = f_{MODEL}(Temp, W, L, V_{GS}, V_{DS}, V_{BS}) \tag{5}$$

where *MODEL* is one of the standard transistor models like BSIM3v3, BSIM4, PSP and EKV. f_W and $f_{V_{GS}}$ are monotonous functions, thus equations (3) and (4) are solved using the Newton-Raphson approach.

Table I gives the definition of the main five classes of the sizing and biasing operators applied to the MOS transistor.

To size and bias a transistor, a bipartite DAG (Directed Acyclic Graph) is associated with it. We have defined a bipartite DAG G(V_p, V_c, A) with the two disjoint sets V_p and V_c. V_p is the set of parameter nodes, V_c is the set of *computation nodes* consisting of operators, and A is the set of arcs that state the dependencies between each operator and its parameters. The bipartite graph [7], [8] for the sizing and biasing of the diode-connected transistor using operator $OPVGD(V_{EG})$ (Table I) is shown in Figure 3.

TABLE I: Class definition of sizing & biasing operators.

Operator	*Definition*
$OPVS(V_{EG}, V_B)$	$(Temp, I_{DS}, L, V_{EG}, V_D, V_G, V_B) \mapsto (V_S, W, V_{TH})$
...	...
$OPVG(V_{EG})$	$(Temp, I_{DS}, L, V_{EG}, V_D, V_S) \mapsto (V_G, W, V_B, V_{TH})$
...	...
$OPVGD(V_{EG})$	$(Temp, I_{DS}, L, V_{EG}, V_S) \mapsto (V_G, V_D, W, V_B, V_{TH})$
...	...
$OPW(V_G, V_S)$	$(Temp, I_{DS}, L, V_D, V_G, V_S) \mapsto (W, V_B, V_{TH})$
...	...
$OPIDS(V_G, V_S)$	$(Temp, W, L, V_D, V_G, V_S) \mapsto (I_{DS}, V_B, V_{TH})$
...	...

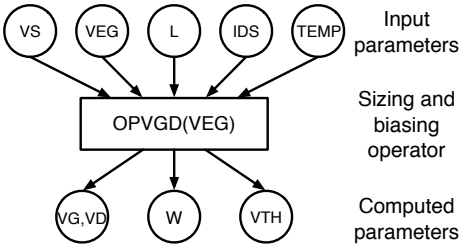

Fig. 3: Graph representing the input parameters and output parameters of the operator OPVGD. [8]

A set of input parameters are defined for the diode-connected transistor. The sizing and biasing operator $OPVGD(V_{EG})$ is then called to compute the set of output parameters. From the bipartite DAG of the transistor shown in Figure 3, more complex bipartite graphs are built for devices which consists of a small set of transistors realizing the primitives of the analog behavior such as differential pairs, cascode, current mirrors [13]. Figure 4(a) illustrates a current mirror device. The designer can set a current ratio of $1:5$ from transistor M_1 to transistor M_2. Therefore the linear constraint $W_2 = 5{*}W_1$ must be respected. The bipartite graph for the current mirror is shown in Figure 4(b). Operator *OPVGD(VEG)* computes the width W_1 for the reference transistor then the designer constraint is added in the graph to compute W_2.

This sizing and biasing methodology is used to generate suitable sizing procedures for circuits that respect the designer's choice of parameters and design constraints. Each sizing procedure for a circuit is a sequence of operators that compute missing sizes and biases, represented as a bipartite DAG. The evaluation of the whole sequence results in the sizes and biases giving the intended DC behavior. This methodology is illustrated by the bipartite DAG shown in Figure 11 for the comparator (Fig. 2). The sizing procedure for the charging and discharging current sources with trimming (Fig. 1) is also built with the same approach.

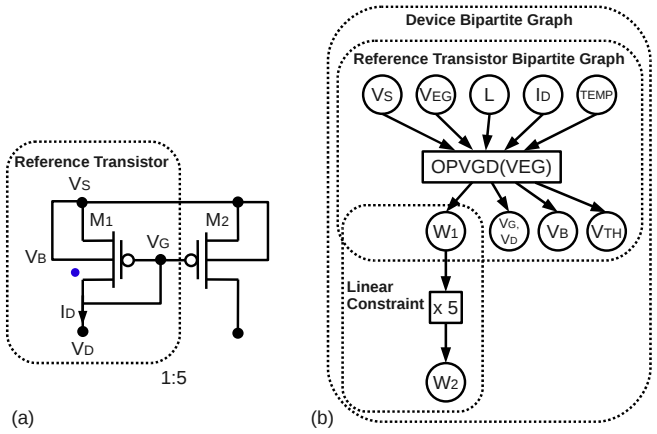

Fig. 4: (a) PMOS current mirror device, (b) its associated bipartite graph. [8]

IV. PROPOSED DESIGN METHODOLOGY

The triangular wave generator consists of two main blocks which are the comparator block and the capacitor charging and discharging block. In the comparator block, the comparator DC node voltages and biasing currents for the comparator are specified in order to have propagation delay less than 10% of the minimum switching period. The transistor sizes are generated using the procedure provided by CHAMS and shown in Fig. 11 to meet the required specifications. A transient simulation of the comparator is performed to evaluate the propagation delay for the comparator. If the specifications are not met, changes in the DC biases are made to modify the transistors aspect ratios. These iterations are done until the specifications are met.

The second block is the capacitor charging and discharging circuit. It comprises the capacitor and the trimming current sources with its associated switches. The capacitor value can be calculated using equation (1) which theoretically is the total capacitance including all the parasitic capacitances at this node for a certain bias current. For the trimming block, the sizing is performed at a certain DC bias voltage to guarantee the proper operation of all the transistors. This ensures that the current sources and switches operate in the saturation and linear regions, respectively. The switches are sized to have a maximum resistance of 50 Ω. Moreover, CHAMS is capable of estimating the parasitic capacitance so the actual value of the load capacitor can be calculated as in the following equation,

$$C_{load}(actual) = C_{load}(calculated) - C_{gg}(comparator) - C_{dd}(MP1,2,3) - C_{dd}(MN1,2,3) \quad (6)$$

where C_{gg} is the total gate capacitance of the comparator input terminal, $C_{dd}(MP1,2,3)$ is the sum of drain capacitances of the transistors MP1, MP2, and MP3, and $C_{dd}(MN1,2,3)$ is the sum of drain capacitances of the transistors MN1, MN2, and MN3. All the circuit components sizes are generated to meet the required biasing and specifications. The error in the frequency is measured. If the error in the frequency exceeds the limits in one process corner, then the trimming range (I_{min}

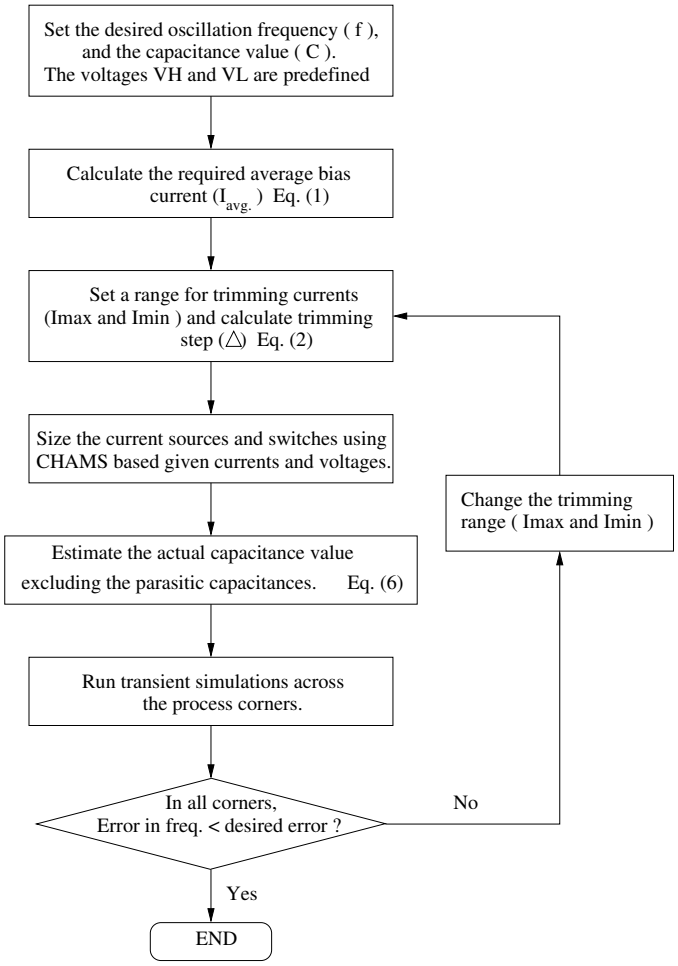

Fig. 5: Current trimming circuit design procedure

and I_{max}) can be modified and transistors are resized again or the capacitor value can be changed. The flow chart in the Figure 5 shows the design procedure for the trimming circuit. This procedure is to maintain a certain frequency with bounded variations across all process corners.

V. Simulation Results

Simulations are performed to verify the validity of the proposed methodology using 0.35 μm CMOS technology. A testbench for the comparator is constructed as shown in Figure 6. A triangular wave with voltage varying from 1.25 V to 3.75 V with frequency of 2 MHz is applied to the negative terminal and a constant voltage of 2.5 V is applied to the positive terminal. The biasing current is 20 μA and the current ratios for the biasing current mirrors are K1 = 5, K2 = 5, and K3 = 10. The transistor sizes are generated by CHAMS (Fig. 11) and iterations are done to obtain a propagation delay less than 3 ns. The resulting propagation delay with rising edge is 2 ns while with falling edge is 2.8 ns as shown in Figure 7. The total power consumption is 1.59 mW.

The design procedure is applied on trimming circuit and simulated for certain process corners. The process corner models in the used technology are shown in Table II.

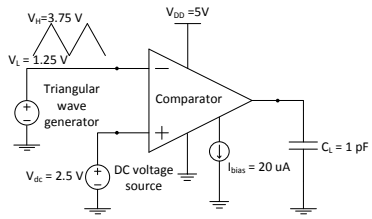

Fig. 6: Comparator testbench to measure the propagation delay

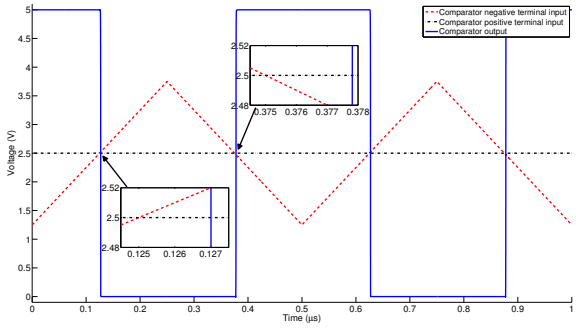

Fig. 7: Comparator input and output signals with indication of rising and falling delays

cmostm	typical NMOS and PMOS
cmosws	worst case speed - slower transistors
cmoswp	worst case power - faster transistors
cmoswo	worst case one - slow PMOS and fast NMOS
cmoswz	worst case zero - slow NMOS and fast PMOS
captm	typical capacitor value
capws	worst case speed - capacitor value greater than typical
capwp	worst case power - capacitor value smaller than typical

TABLE II: CMOS process corners definition in CMOS $0.35\mu m$

Combination of the transistor and capacitor process corners is illustrated in Table III and numbered to be used in the succeeding results. The procedure for trimming is done for oscillation frequency of 2 MHz. Using the current trimming, the variations in the frequency are kept within $\pm 3\%$ error across all process corners. As shown in figure 8, the solid lines represent the desired nominal oscillation frequency and the dashed lines represent the minimum and maximum acceptable range of frequency variations. The capacitor value used is 3.63 pF after excluding the parasitic capacitances. The minimum and maximum currents are 35 μA and 47 μA, respectively. The step in the trimming current is 4 μA. Thus, The trimming currents are 35 μA, 4 μA, and 8 μA.

Corner number	1	2	3	4	5	6	7	8	9
capacitor model	tm	wp	ws	wp	ws	wp	ws	tm	tm
CMOS model	tm	wp	ws	wo	wo	wz	wz	wo	wz

TABLE III: Process corners models used in simulations

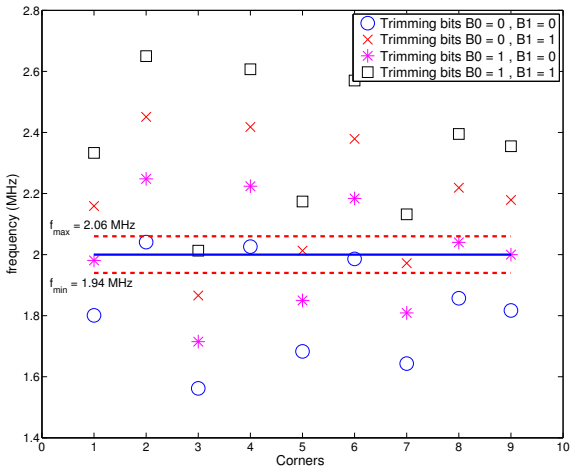

Fig. 8: Oscillation frequency variation with process corners. The desired frequency is 2 MHz. Using B0 and B1, the desired frequency is obtained with error $\pm 3\%$ maximum.

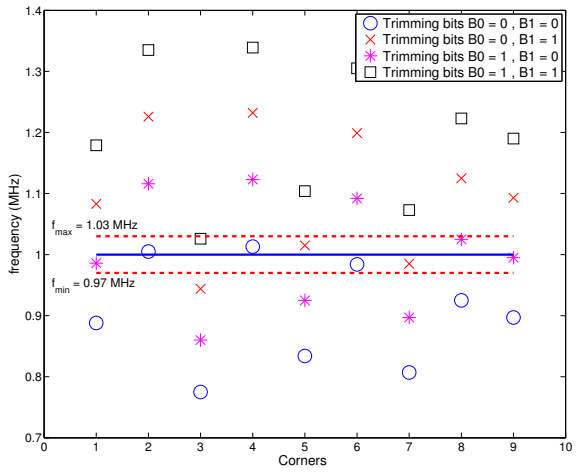

Fig. 9: Oscillation frequency variation with process corners. The desired frequency is 1 MHz. Using B0 and B1, the desired frequency is obtained with error $\pm 3\%$ maximum.

The same procedure is repeated for different oscillation frequencies 1 MHz and 4 MHz. Table IV shows a summary of the specification for the different trimming circuits. The frequency variations versus the process corners for the frequencies 1 MHz and 4 MHz are shown in Figures 9 and 10, respectively.

Oscillation frequency	1 MHz	2 MHz	4 MHz
Error	$\pm 3\%$	$\pm 3\%$	$\pm 3\%$
Trimming minimum current	$17\mu A$	$35\mu A$	$35\mu A$
Trimming maximum current	$23\mu A$	$47\mu A$	$47\mu A$
Trimming current step	$2\mu A$	$4\mu A$	$4\mu A$
Capacitor	3.78 pF	3.63 pF	1.63 pF

TABLE IV: Trimming circuits specifications for different oscillation frequency

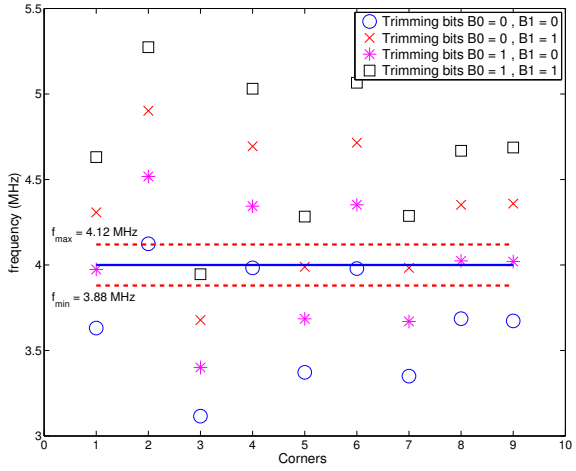

Fig. 10: Oscillation frequency variation with process corners. The desired frequency is 4 MHz. Using B0 and B1, the desired frequency is obtained with error $\pm 3\%$ maximum.

VI. Conclusion

A systematic design methodology for a triangular wave generator has been proposed. The proposed methodology is employing a sizing tool developed in LIP6-UPMC called CHAMS. It is used to size the transistors of the comparator and the trimming current sources and its switches. The trimming circuit is designed for different oscillation frequencies (1 MHz, 2 MHz, and 4 MHz) with a maximum frequency variation of $\pm$ 3% across nine process corners in CMOS 0.35 μm.

The key advantage of the proposed methodology is the flexibility in choosing the oscillation frequency and resizing the trimming circuit with less design time. Moreover, the proposed flow can be used for different technologies with limited modifications.

Acknowledgment

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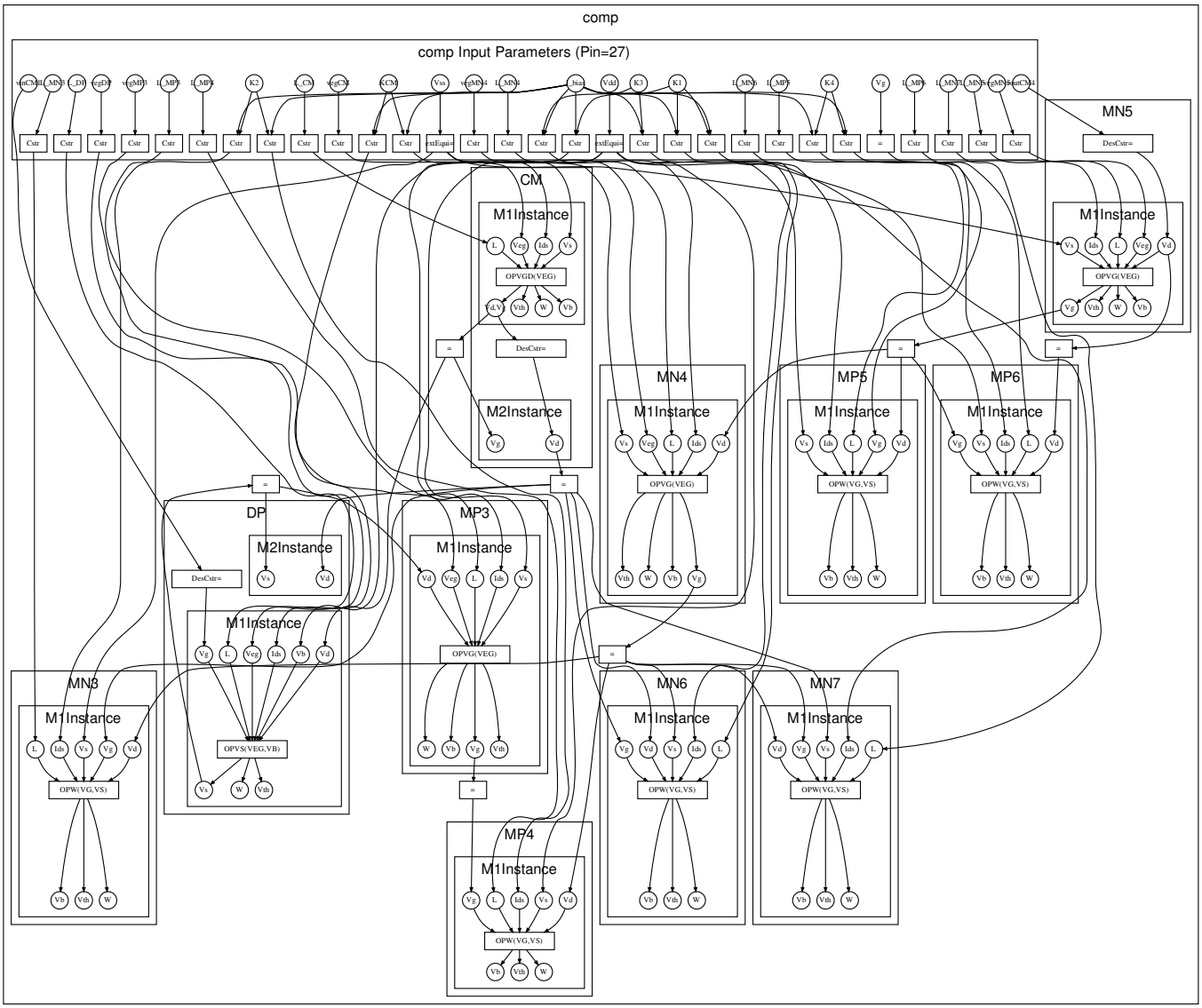

Fig. 11: Bipartite DAG of the comparator provided by CHAMS