

Substrate Modeling to Improve Reliability of High Voltage Technologies

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Abstract—In Smart Power ICs there is the need of new substrate models to be integrated in the design flow of power circuits. This work reports the latest results regarding the substrate modeling methodology based on three-dimensional lumped components extraction of diodes, resistors and contacts. The substrate network including lateral and vertical parasitic bipolar transistor can be automatically created from any chip layout including temperature and geometry variations. In such a way fast dc and transient analysis can be carried out in early design stages to improve reliability of high voltage ICs. Since the high variability and complexity on modern Smart Power technologies, a flexible model is required. This work discusses all the features related to technology variations. Circuit simulator results are then compared with TCAD simulations.

I. INTRODUCTION

Substrate related problems are subject of study since 80s from mixed-signal circuits. Specific design guidelines based on proper layout rules and guard rings placements have been developed for designers in order to minimize undesired effects [1]. However, after the silicon production parasitic problems can still arise. In particular, in Smart Power ICs which integrate on the same chip low-voltage and high-voltage transistors, the switching of typical inductive load will cause current injection into the substrate compromising the chip functionalities. For this reason, in case of high-voltage CMOS technologies, foundries provide today additional guidelines to reduce the coupling due to minority carriers. These guidelines are based on measurements of distributed bipolar transistor to estimate the coupling current variations with distances [2]. However, this approach is not accurate since it does not take into account more complex layouts typical of real ICs which can results in increased coupling mechanisms.

In the last 20 years scientific community is particularly focused on finding new solutions for protecting chips, especially in Smart Power technologies. As a matter of fact, the only way to simulate such complex phenomena is by the use of Technology Computer Aided Design (TCAD) software. In this software the equations of semiconductors physics are numerically solved using Finite Element Method (FEM) leading to accurate results. The drawback is the enormous amount of computer resources and time that is required to perform such simulations. This is then a solution that designers do not normally use. In any case it is important to mention that some works have used TCAD as the main tool to develop protections for minority carriers injection in order to reduce the substrate

cross-talk [3], [4]. Other options normally used to reduce the substrate parasitic couplings are based on technological modifications, like improved isolation structures or the use of Deep Trench Isolation (DTI) structures [5].

A part from protection design, TCAD has been also used to analyze failure mechanisms in substrate of Smart Power circuits. The best example is the project SUBSAFE in 2001 [6]. In the framework of this project it was shown that the minority carrier injection from a H-bridge circuit can be efficiently simulated with TCAD. Today, this is also the only existing approach for transient simulation of substrate currents.

A part from FEM tools other numerical techniques have been used to address the problem of substrate current simulation and to drastically reduce the simulation time down to seconds. A proposed approach is to use Green's function to solve the 3D diffusion equation of minority carriers in the substrate [7]. This option requires a complex mathematical formulation that cannot be easily extended to more complex problems or geometries when drift current has an important role and it requires a dedicated software that cannot be integrated with actual circuit simulators and Process Design Kits (PDK) of foundries. On the other side, the most promising approach to integrate minority carriers simulation in circuit simulators is the one proposed by Oehmen et al. [8]. It consists to mesh the substrate in spheres and solve the semiconductor equations by means of Kirchhoff laws. The basic polar diffusion equation solution is added in the model and then the coupling currents are computed as linear combination of all the injected carriers. However, this approach is limited to simple circuit configurations.

A similar approach was proposed by EPFL [9] based on finite difference scheme in a rectangular mesh. The proposed solution takes into account the minority carriers diffusion at circuit level and it is based on a semi-analytical approach which involves equivalent voltages and currents defined to find the solution by spice-like simulators. It was shown [10] that a circuit made of connection of several of these devices can efficiently simulate the minority carriers' contribution to the coupling currents in Smart Power ICs. This substrate modeling methodology will be further exploited in this work showing its flexibility to model any high voltage technology.

To apply the model for a three dimensional geometry, the entire chip is divided in smaller parts defining a three dimensional grid of intermediate nodes. This "meshing strat-

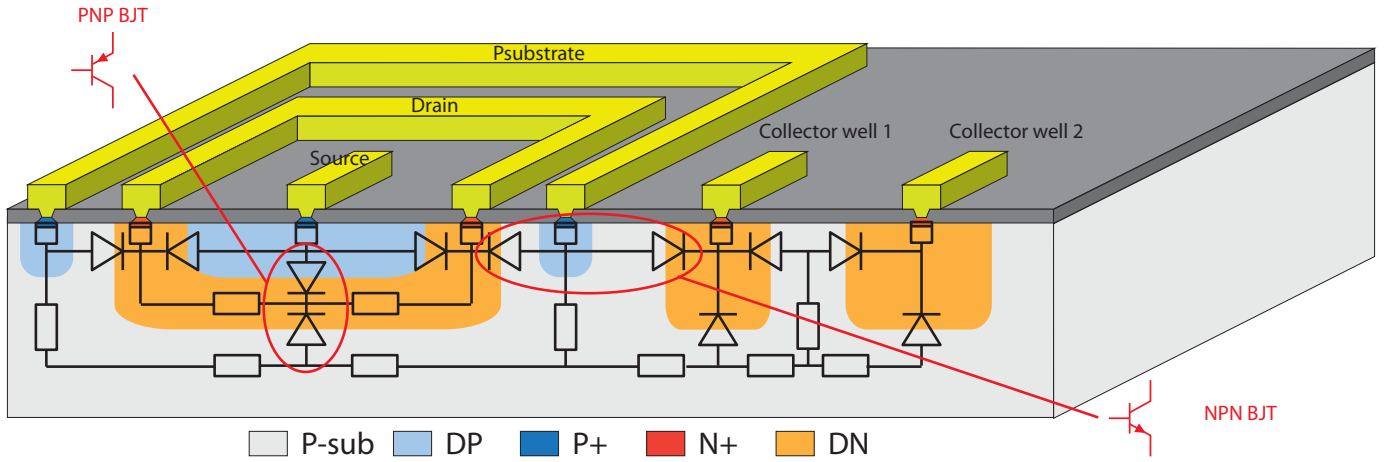


Fig. 1. Cross section of a High Voltage technology showing the parasitic vertical PNP of a LDMOS and the parasitic lateral NPN with nearby collecting wells. The substrate network can be modeled by the interconnection of diodes, resistors and contact including minority carriers propagation.

egy” is layout dependent. Between the different nodes, the EPFL resistances and the EPFL diodes are used to create the equivalent parasitic network to be simulated. As a result, the EPFL Substrate Model is an extension of mixed signal RC substrate noise models [11] with the capability to simulate also the minority carriers’ effects. For example, even if the model does not include any bipolar transistors (BJT), the connection of different EPFL diodes is able to predict the presence of eventual parasitic BJT (see Fig. 1). While for classical substrate noise analysis in mixed-signal circuits several tools have been developed, no tools are today available to automatically extract the parasitic substrate network for Smart Power IC including BJTs.

The simulation of this network requires much less time and computational resources than FEM simulations representing and interesting tool for designers in the early stages of the design flow. The potentialities of this approach have been shown by Lo Conte et al. [12] for the simulation of below-ground condition of a full H-bridge circuit.

This paper is organised as follows: in Section II the components of the proposed substrate model are described; in Section III the modeling methodology is reported discussing how several high voltage technology variations can be easily simulated. Finally, in Section III TCAD simulations are compared with circuit results while conclusion is reported in Section V.

II. SUBSTRATE CURRENT MODEL

As shown in Fig. 1, common CMOS technologies include MOS and LDMOS devices on a P-doped substrate with several N and P wells corresponding to the drain/source of other devices or used as isolation rings. The combination of different PN junctions results in several BJTs with different geometry and gain. These devices can be triggered on during transient operation of high power stages injecting carriers into the substrate which propagate disturbing nearby circuits. The coupling currents can be simulated with the corresponding

substrate circuit.

The IC substrate can be modeled with a parasitic network of three lumped components: the EPFL diode, the EPFL resistance and the the EPFL homojunction. This network is highly dependent on the chip layout and can be automatically extracted processing the used mask layers [13]. Across PN junctions a diode is instantiated which injects or collects minority carriers, in the bulk substrate resistances are used to propagate the charges while at PP+ NN+ doping discontinuities the homojunction model is used. This process results in a three-dimensional parasitic netlist that can be backannotated with the top metal routing allowing the full-chip simulation of the circuit. Back-to-back connection of two diodes is equivalent to the parasitic NPN lateral BJT while the front-to-front connection simulates the vertical PNP BJT. This is possible because the diode and resistor models are enhanced with two additional terminals allowing the propagation of minority carriers into the silicon volume.

Since no closed form solution can be obtained for the drift diffusion equations of minority carriers, the model of each components is obtained by finite difference scheme analysis in one dimension. The resulting models include temperature variation and are independent on the applied voltages, then suitable from low to high voltage devices. The equivalent circuit models are reported in Fig. 2 and consist in two coupled circuits [14]. The total current circuit (TCC) for voltages and currents includes the substrate resistance modulated by minority carriers injection. The minority carrier circuit (MCC) for the propagation of electrons or holes is based on equivalent voltages V_{eq} proportional to minority carriers concentration and equivalent currents I_{eq} proportional to their gradient. In the MCC the resistive Π -network models the drop of concentration, while the controlled current sources are the correction drift terms of the electric field to diffusion. In case of the homojunction a non-linear voltage drop of minority carriers concentration is included [15], while for PN junctions, controlled voltage sources model the exponential injection of

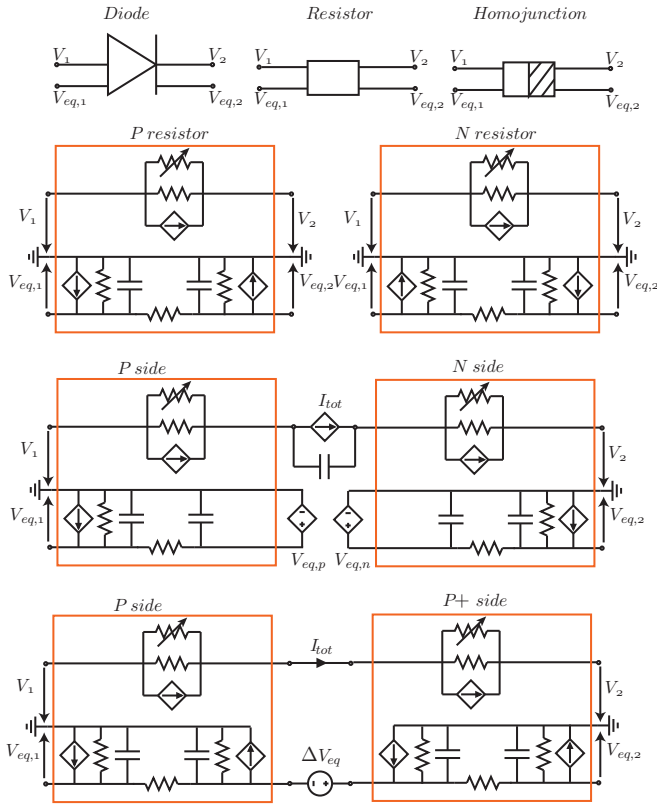


Fig. 2. Diode, resistor and homojunction lumped element symbols with corresponding equivalent circuits for total current (TCC) and minority carriers (MCC).

carriers.

Capacitive components are also added in the depletion region of PN junction as the standard spice junction capacitance, and diffusion capacitances related to the distributed charge of minority carriers are added to the MCC [16]. This allows to have the complete model for transient and AC analysis covering low- and high-injection levels of minority carriers including the modulation of substrate resistance. The threshold between the two regimes is around the built-in voltage of the junction.

III. TECHNOLOGY VARIATIONS

Fig. 3 shows four separate cross sections of a test structure with two N-wells placed at a fixed distance in a P-type substrate, each with a different substrate doping profile and isolation type. Each test structure can be biased in order to activate the lateral parasitic NPN device which couples the two N-wells through the substrate. Electrons injected at the emitter side which do not recombine into the substrate, are collected when passing close to the collecting diode junction. P-type substrates contacts are placed between two N-wells to provide majority carriers recombination.

Fig. 3a shows a simplified cross section with two high voltage N-wells in a low and uniformly doped P-type substrate. This structure exists in junction isolated high voltages technologies based on standard high voltage CMOS processes

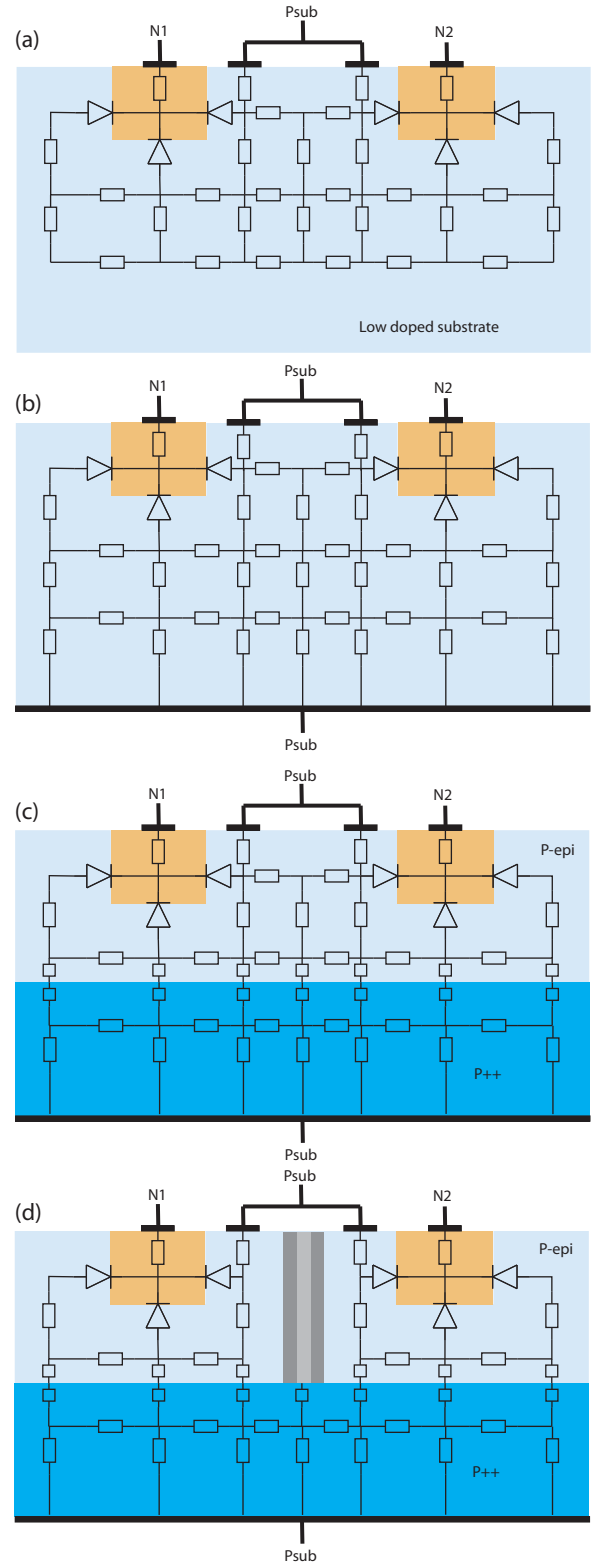


Fig. 3. Cross section of two N-wells in different technologies and corresponding equivalent circuit: (a) HVC MOS with low doped substrate; (b) backside contact; (c) P++ substrate with epi-layer; (d) DTI technology option.

(HVC MOS), where extra masks are added to build HV devices and ensure the electrical isolation from each other [17]. The

presence of back-side metallization is a common option (Fig. 3b), where additional substrate ohmic contacts are added to the back side of the wafer to ensure a uniform ground potential to the substrate. The equivalent substrate model consists in a network of diodes, to model PN junctions, diffusion P-type resistors, to model the substrate and homojunctions to model both N-wells and substrate contacts (see equivalent model in Fig. 3a). To model the backside connection, an additional row of P-type diffusion resistors has been added at the bottom side of the model network (see equivalent model in Fig. 3b). Note that this simplification neglects the effects of the backside Schottky barrier on the back side contacts [6].

Besides HVCMOS technologies, also bipolar CMOS LD-MOS (BCD) processes are used for high voltage. BCD technologies provide an epitaxial type of substrate along with the wafer back side connection. In this case, a thin lightly P-doped silicon epitaxial layer is grown on a heavily P++ doped silicon wafer. Fig. 3c shows a simplified cross section with two high voltage N-wells in a P-/P++ substrate. The P-/P++ discontinuity forces the minority carriers to flow laterally in the P- region instead of down into the substrate, minimizing the overall couplings due to minority carriers [18]. In this particular case, homojunctions are used to model the P-/P++ substrate discontinuity in the substrate model (see equivalent model in Fig. 3c).

Often, dielectric isolation is used to further minimize the couplings in BCD high voltage processes [19]. Fig. 3d shows a simplified cross section with two high voltage N-wells in a P-/P++ substrate with deep trench isolation. The injected electrons flow is forced deep into the P++ substrate, where they recombine with a higher recombination rate. Therefore the total amount of collected charge is reduced. For DC simulations, deep trench isolation (DTI) is modeled as a cut in the substrate network (see equivalent model in Fig. 3d).

IV. MODEL RESULTS

The proposed model blocks are coded in VerilogA, integrated in the Cadence design flow environment and simulated by Spectre circuit simulator. Results are compared with TCAD Sentaurus device software simulations for different structures.

In Fig. 4 an example of multi-collector lateral NPN BJT is reported. The structure is composed by three N wells (with an area of 0.0144 mm^2) in a low doped P substrate with slightly different distances (N1 N2 are $71 \mu\text{m}$ apart while N2 N3 are $80 \mu\text{m}$ far away) thus it is not symmetric. When the centered well, which represents for example the drain of a high voltage transistor, goes below ground condition, minority carriers are injected into the substrate activating the parasitic transistor current paths. The electrons propagates into the substrate by diffusion reaching the nearby wells. These substrate couplings can be simulated with the corresponding equivalent circuit reported in Fig. 4. As shown in Table I for -0.5V on N2 the model is able to track the small difference in coupled currents due to the asymmetry of the configuration with an error of around 30%. This allows designers to rapidly check in

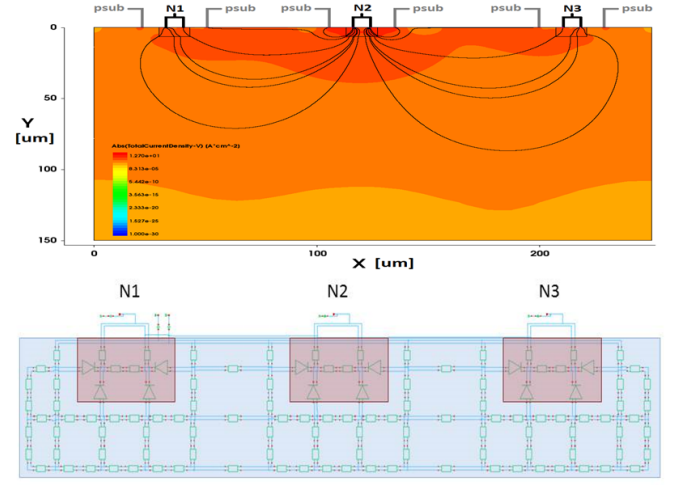


Fig. 4. TCAD simulation of three N-wells in P substrate (top) with corresponding substrate parasitic network (bottom). Color plot corresponds to the current distribution for below ground condition of the centered well.

TABLE I
SIMULATION RESULTS FOR THE MULTI-COLLECTOR BJT OF FIG. 4.

	N1 @ 50V	N2 @ -0.5V	N3 @ 50V	PSUB @ 0V
TCAD	$9.5 \mu\text{A}$	$-41.0 \mu\text{A}$	$8.5 \mu\text{A}$	$2.3 \mu\text{A}$
VerilogA	$11.9 \mu\text{A}$	$-41.6 \mu\text{A}$	$11.6 \mu\text{A}$	$1.8 \mu\text{A}$
Error	25 %	1.5 %	37 %	21 %

circuit simulator the best distance to avoid unintended coupling currents.

Moreover, the model can be applied also to different technologies as described in Section III. As example we report the study on the coupling between two N wells $20 \times 100 \mu\text{m}^2$ when one well goes below ground and the other is biased at 12 V . Two conditions are reported in Table II comparing the current of the parasitic NPN BJT: -0.5V (low electron injection) and -0.8V (high electron injection where the coupling $\alpha = I_C/I_E$ is maximum). Simulated electron concentration plot in TCAD for the five selected geometries are reported in Fig. 5 and circuit model well matches with physics simulator results.

For simple HVCMOS technologies (geometry 1) the two wells with average doping $1 \times 10^{17} \text{ cm}^{-3}$ are placed inside a low doped substrate ($1 \times 10^{15} \text{ cm}^{-3}$) at $50 \mu\text{m}$ distance. This results in a coupling ranging from 0.4 to 0.8. In this case no backside contact is considered. In geometry 2 the backside metallization is added showing no changes in the couplings. However, for the high injection condition when 2.5 mA are injected into the substrate the geometry 1 reports a maximum substrate shift of 124 mV while geometry 2 only of 63 mV .

Geometry 3 has been modified in order to study the effect of high doped substrate ($5 \times 10^{18} \text{ cm}^{-3}$) with a P- epi layer of $15 \mu\text{m}$ thickness. In this case both currents and couplings are strongly affected. In general lower currents are injected but the overall coupling between the two wells is strongly increased. This is due to the reflection of electrons to the PP+ interface. In geometry 4 a simple deep trench is placed showing how

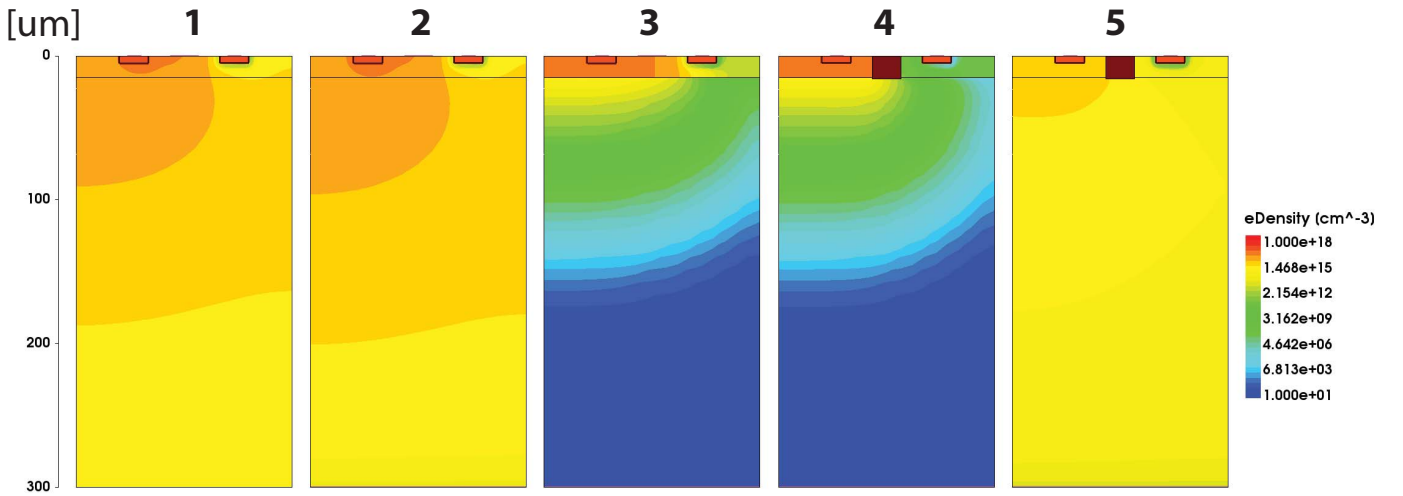


Fig. 5. Electron density color plot from TCAD simulations of five different structures for -0.5V below ground condition: (1) low-doped substrate of HVMOS, (2) low-doped substrate with backside contact, (3) P++ substrate with epi-layer and backside contact, (4) P++ substrate with epi-layer, DTI and backside contact, (5) DTI isolation in low-doped substrate with backside contact.

TABLE II

TCAD (TOP LINE) AND CIRCUIT (BOTTOM LINE) RESULTS FOR TWO DIFFERENT BELOW GROUND CONDITIONS IN THE FIVE TECHNOLOGY CONFIGURATIONS OF FIG. 5.

-0.5V	1	2	3	4	5
I_E	1.73 μA 1.38 μA	1.76 μA 1.40 μA	0.59 μA 0.50 μA	0.13 μA 0.10 μA	1.42 μA 1.24 μA
I_B	0.99 μA 0.86 μA	1.02 μA 0.88 μA	0.15 μA 0.14 μA	0.13 μA 0.10 μA	0.96 μA 0.83 μA
I_C	0.74 μA 0.52 μA	0.74 μA 0.52 μA	0.44 μA 0.36 μA	5 pA 4 pA	0.46 μA 0.41 μA
α	0.43 0.38	0.42 0.37	0.75 0.72	4e-5 4e-5	0.32 0.33
-0.8V	1	2	3	4	5
I_E	2.40 mA 2.19 mA	2.66 mA 2.45 mA	1.84 mA 2.00 mA	0.38 mA 0.32 mA	0.24 mA 0.23 mA
I_B	0.73 mA 0.69 mA	0.99 mA 0.98 mA	0.45 mA 0.35 mA	0.38 mA 0.32 mA	0.17 mA 0.17 mA
I_C	1.67 mA 1.50 mA	1.67 mA 1.47 mA	1.39 mA 1.65 mA	8 nA 197 nA	0.07 mA 0.06 mA
α	0.69 0.68	0.63 0.60	0.75 0.82	2e-5 6e-4	0.29 0.26

V. CONCLUSION

The substrate of Smart Power ICs can be modeled by an equivalent parasitic network composed of diodes, resistors and contacts whose spice-like model is coded in VerilogA. These devices have additional two-terminals to propagate minority carriers and to allow simulation of parasitic PNP and NPN bipolar transistors. Their placement and dimensions strongly depends on layout and technology constraints. An automatic meshing algorithm can be developed to compute the required parameters and interconnection starting from the circuit layout and backannotating the substrate netlist to the original circuit. The simulation of the final netlist is then easily integrated in standard design flows of IC and it allows to fast simulate multi-collector couplings in short times. Technology variations as the placement of deep trenches or backside contact are easily handled by the proposed substrate methodology. Comparison between TCAD and equivalent circuit simulation are in good agreement and show how the model is able to track the current coupling variations as a consequence of isolation structures, substrate doping and electrical configurations.

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it definitively kills the coupling forcing minority carriers to recombine in the P++ substrate. This technology modification is highly efficient only if the P++ substrate is present. To show this, geometry 5 reports the same DTI structure without the highly doped substrate. With respect to geometry 2 only a small factor on current couplings is gained in this way.

In conclusion, the model is able to track all the different geometry options and to evaluate which is the best solution regarding a particular circuit with few second simulation.

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