Substrate noise modeling with dedicated CAD framework for smart power ICs

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Abstract—In smart power IC technology, low and high voltage circuits are integrated on the same substrate. The commutation of the high voltage circuits can induce substrate parasitic currents which can severely disturb the operation of the low voltage circuits. The parasitic currents due to minority carriers in the high voltage technology can be significantly high. However, the minority carrier propagation into the substrate is not considered in most of existing circuit simulators. In this paper, a novel computer-aided design tool for substrate parasitic extraction is proposed. A simple circuit with an injecting and a collecting N-wells over a P-substrate is studied. With the distance between the wells varying, the lateral bipolar effect is illustrated. The spectre simulation results of extracted substrate equivalent circuit are compared to a TCAD simulation results. The comparison shows an acceptable relevant error. However, the simulation time was reduced by approximately 1400 times with respect to the TCAD.

I. Introduction

Integration of low voltage circuits with high voltage devices is used in smart power IC design [1]. However, unexpected substrate parasitic noise can severely disturb the sensitive nearby low voltage devices during the switching of power stage. Such substrate-noise coupling is considered the major cause of failures inside smart power integrated circuits [2]. The minority carriers propagation is still unpredictable and can cause failure after fabrication. This may increase the number of redesigns needed, increasing the cost and time-to-market [3].

Experimental extraction methodology of substrate-noise coupling was proposed in [4]. It is based on predicting a simple equivalent circuit from layout, or during conventional circuit simulation. However, it is not convenient for a complex circuit layout and lacks in accuracy. Today, none of the existing extraction methodologies consider minority carriers diffusion in the substrate of integrated circuit. Technology Computer-Aided-Design (TCAD) [5] tools are the only tools available to interpret the impact of minority carriers. Despite physical based computer simulation are accurate, these are yet time-consuming [6].

In this paper, we extend the substrate modeling approach initially proposed in [3], [7]. We show that this approach can be easily used to model lateral parasitic bipolar effects that accounts for minority and majority carriers propagation in the semiconductor substrate. An equivalent electrical schematic for the substrate is extracted by using a dedicated parasitic extraction tool. To illustrate the effectiveness of the approach, a layout with one injecting and one collecting N-wells over a P-substrate in studied. Results of circuit simulation is compared to a three dimensional TCAD simulation. The comparison shows that circuit simulation is very fast compared to TCAD simulations with an accuracy that is still quite acceptable.

The paper is organized as follows, in Section II a description of substrate parasitic models are illustrated. In Section III the architecture of extraction tool is presented. Comparison between circuit simulation of extracted substrate and TCAD simulation is discussed in Section IV. Finally conclusions are drawn in Section V.

II. Modeling methodology

Fig. 1 shows a typical circuit configuration of Smart Power ICs. A 50V power NDMOS is used as output transistor with a load connected to its drain. During the circuit switching this node goes below ground forward biasing the drain N-well. Electrons are then injected in the substrate and are collected by nearby devices, as the isolation well of low-voltage NMOS. The resulting parasitic lateral NPN is difficult to characterize because its electrical characteristics are dependent on the distance W_b between the two devices which is layout dependent. This distance corresponds to the substrate base of the parasitic BJT. To be able to simulate this coupling mechanism in standard design-flow an equivalent substrate network should be
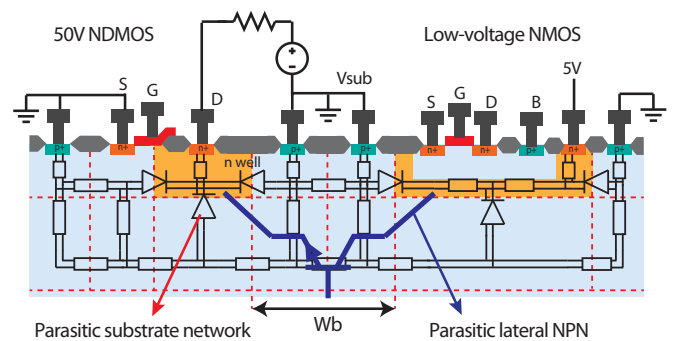

Fig. 1: Substrate equivalent circuit to model parasitic lateral NPN between high-voltage aggressor and low-voltage victim devices.

extracted. This network cannot include compact model BJTs because their current gain is unknown and layout dependent. As proposed by [8], the extracted substrate circuit could be composed indeed of only diodes and resistances if minority carriers propagation is taken into account. The extraction of the substrate network should be done in an automatic way processing a general three-dimensional layout. The substrate must be divided in blocks (see red dashed lines in Fig. 1) and diodes or resistances should be properly instantiated. As a consequence, the parasitic lateral bipolar can be easily simulated if analyzing the layout we are able to detect PN junctions as injection or collector points of electrons, and to propagate the carriers through their interconnection by the means of diffusion resistances. The fundamental devices to consider for substrate currents modeling are then 4-terminal diodes and resistors able to carry physical voltages V and currents I but also minority carriers concentration (additional voltage V_{eq}) and gradient (additional current I_{eq}).

III. CAD TOOL FOR SUBSTRATE SIMULATION

The proposed methodology for substrate modeling relies on a 3D network of interconnected substrate parasitic components to represent the equivalent electrical substrate network. The principal idea is based on constructing a three dimensional meshing network, which is modeling the substrate by cuboid elements. Rectilinear layout-based meshing strategies are implemented to ensure minimum meshing for the extracted layout.

The diagram representing the substrate noise modeling flow using automatic extraction is depicted in Fig. 2. The entire CAD framework is developed by using "OpenAccess" [9] open source API. As reported in [6], the accuracy of substrate-noise modeling is strongly dependent on the number of extracted parasitic components and its impact on the simulation time. At this first trial, we assume that minimal number of components is generated since the meshing is chosen to be minimal.

A. Pre-processing stage

Conventional extraction rules designed for substrate parasitic extraction have been introduced in [7]. In this work, a proposition of substrate extraction rules for the case studying is described as followings:
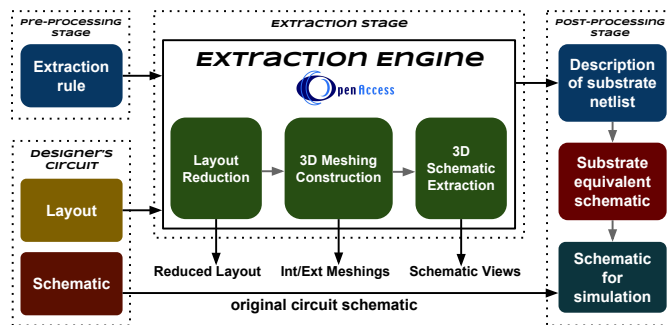

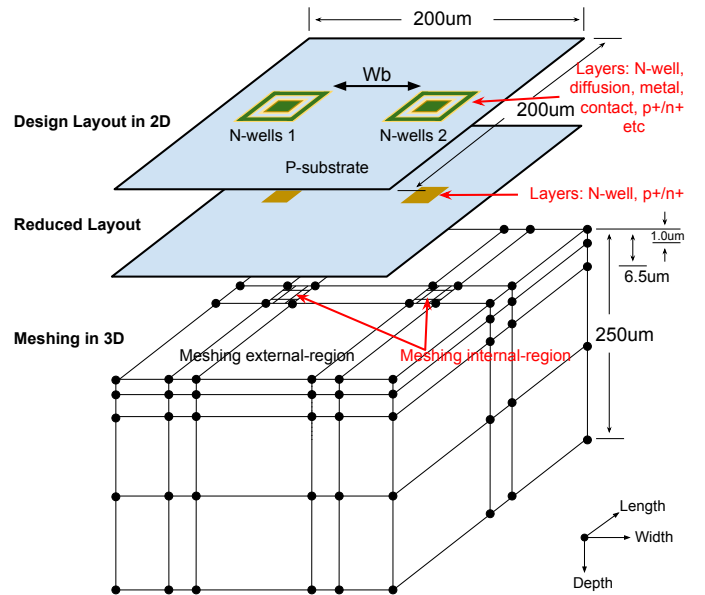Fig. 2: The overall substrate parasitic extraction flow.

Fig. 3: Pre-processing of design layout.

- *Layout reduction mechanism*. Declare the layers not contributing to substrate parasitic, with *"bypass"* operation. It will actually neglect the indicated layers from layout database during extraction process and produce a reduced version of layout as presented in Fig. 3. Only N-well layer is considered contributing to substrate parasitic in this simple case. Otherwise, p+/n+ layer are related to homo-junction contact extraction [10].
- *Definition of well-section*. Consider the layout-dependent specifications given in Tab. I. Four well-sections are defined in "depth" direction (see mesh in 3D in Fig. 3). User-define extraction rules specifying the depth of each well-section are proposed in Tab. II, e.g. the depth of top well is $1.0\mu m$, considering the p+/n+ homo-junction contact, which is actually the half of the depth to cuboid (from center to edge).

TABLE I: Layout-dependent specifications

Layer	Length (for one)	Width (for one)	Depth
p+ (polygon)	$34.9\mu m$	$34.9\mu m$	$0.5\mu m$
n+	$20.1\mu m$	$20.1\mu m$	$0.5\mu m$
N-well	$20\mu m$	$20\mu m$	$6.5\mu m$
P-substrate	$200\mu m$	$200\mu m$	$250\mu m$

TABLE II: User-define extraction rules

Well-section	Depth	Layers
top	$1.0\mu m$	p+, n+, N-well
bottom1	$5.5\mu m$	N-well
bottom2	$100.0\mu m$	(P-substrate)
bottom3	$143.5\mu m$	(P-substrate)

(a) top-layer for $W_b = 20\mu m$ (b) top-layer for $W_b = 60\mu m$ (c) focus on well region of (a)   (d) bottom2-layer for $W_b = 20\mu m$
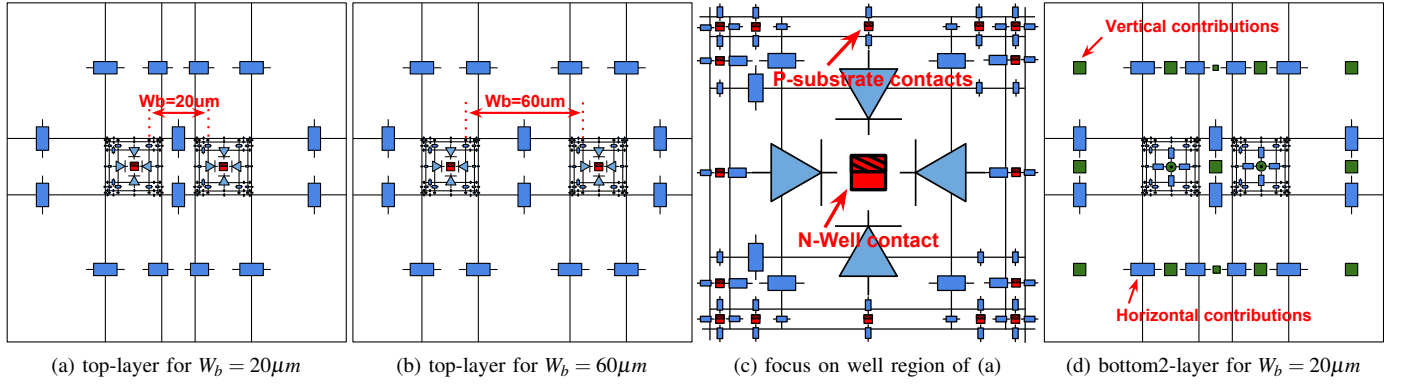
Fig. 4: Comparisons of meshing in 2D for $W_b = 20\mu m$ (a) and $W_b = 60\mu m$ (b) distance between the two wells, and extracted parasitic component for top-layer (a, b), N-well region (c) and bottom2-layer (d).

B. Extraction stage

At extraction stage as illustrated in Fig. 2, consider the *OpenAccess* layout database and conventional user-defined extraction rules as inputs. Then automatic extraction is performed on three steps as following:

- Layout reduction mechanism is performed at this moment and produce a reduced version of layout as illustrated in Fig. 3: N-well layer and p+/n+ layers are considered to have contributions to meshing network. This reduction mechanism saves significantly the computation time during extraction phase of large-scale integrated circuit.
- Meshing strategy relies on a three dimensional meshing strategy after scanning the reduced layout. Figures 4a and 4b represent the meshing in 2D for different spacing between two N-wells (mesh rectangles in Fig. 4a for $W_b = 20\mu m$ and Fig. 4b for $W_b = 60\mu m$).
- Component extraction mechanism is performed by going through the complete meshing in 3D and examining the neighbouring cuboids for horizontal and vertical contributions. Results of extraction are illustrated in Fig. 4. The blue resistance/diode components shown at Figures 4a, 4b represent the extraction horizontal for top layer. If we focus on the well region as Fig. 4c is presenting: four diodes are extracted surrounding N-well which is over a P-substrate, homo-junction contacts are extracted where the *"p+"* or *"n+"* present (see red rectangles). Vertical contributions are seen in bottom layer-sections which create the connection to the layer above. E.g. green rectangles in Fig. 4d represent the vertical resistances between bottom2-layer and bottom1-layer.

C. Post-processing stage

A CADENCE Design Systems [11] description language (SKILL) based program is embedded in CADENCE, and designated for components instantiation and placement of the complete substrate parasitics in the schematic environment during post-processing stage. The schematic can be simulated with a circuit simulator to see the effect of substrate noise.

For the purpose of further investigations, future developments will back-annotate the extracted substrate circuit to the original circuit.

IV. PARASITIC LATERAL NPN

SPICE and TCAD simulations results were compared in order to validate the substrate model and the CAD extraction tool. Two three-dimensional structures (Fig. 5) including an injecting and a collecting N-well over a P-substrate representing the parasitic NPN lateral transistor commonly encountered in Smart Power ICs were studied.

The common p-type substrate for both structures is a cube with dimensions L=200μm by W=200μm by H=250μm. Both structures include two centred n-type wells placed at different distance: n-well spacing of $W_b = 20\mu m$ and $W_b = 60\mu m$ in the first and second structure. All n-type wells are the same with dimensions L=20μm by W=20μm by H=6.5μm and they are surrounded by a p+ doped ring 10μm wide. Each n-type well is connected out by a n+ diffusion covering the entire well.

The P-substrate doping density profiles was assumed constant and equal to Na=$4.5 \cdot 10^{15} cm^{-3}$. The n-wells doping density profiles were assumed to be Gaussian with peak doping density of $2 \cdot 10^{17} cm^{-3}$ and junction depth of 6.5μm. In
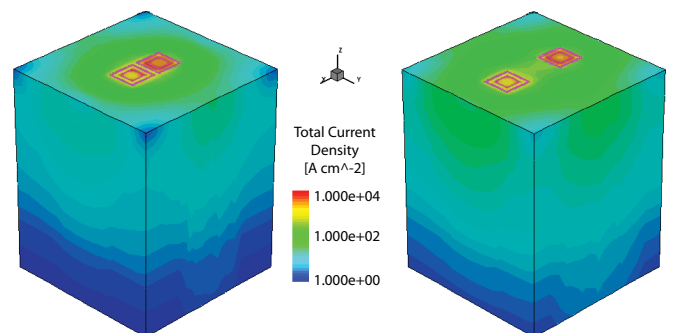

Fig. 5: Total current density from TCAD simulations at $V_{N1} = -1V$ and $V_{N2} = 5V$ for $W_b = 20\mu m$ (left) and $W_b = 60\mu m$ (right) distance between the two wells.
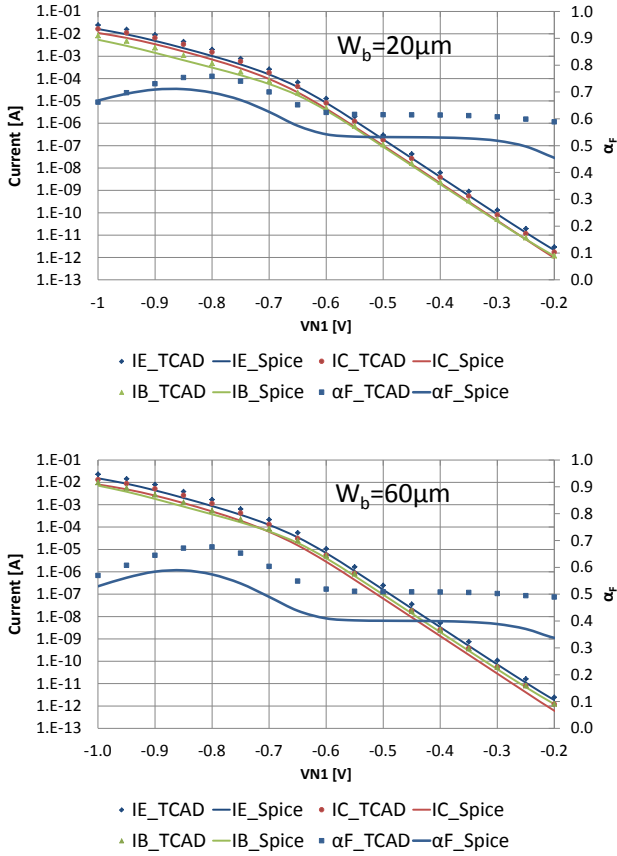
Fig. 6: comparison of simulated NPN Gummel plot with $V_{N2} = 5V$ for $W_b = 20\mu m$ (left) and $W_b = 60\mu m$ (right) distances.

the same way, doping density profiles for p+ and n+ doped diffusions were assumed to be Gaussian with peak doping density of $5 \cdot 10^{19} cm^{-3}$ and homojunction depth of $0.5\mu m$.

Using 3D Synopsys Sentaurus device simulator, the lateral NPN bipolar transistor gummel plot was derived. With the p-substrate biased at 0V and the collector VN2 biased at 5V, the emitter voltage VN1 was swept from 0V to -1V in order to activate the lateral NPN transistor. A lumped element resistance of 2Ω was tied to the emitter, base and collector terminal to mimic practical circuit metal connections.

The equivalent substrate netlists were extracted from both layouts to set up 3D SPICE simulations. Since the equivalent substrate model assumes abrupt p-n junction, the doping

		Number of Meshing Elements	Number of DC Points	Simulation time [s]
Layout Wb=20um	TCAD	325000	21	2 hours
	SPICE	510	101	5 sec.
Layout Wb=60um	TCAD	320000	21	2 hours
	SPICE	510	101	5 sec.

TABLE III: TCAD and SPICE simulation time comparison

concentration parameters used in the substrate electrical model are constant and equivalent to the averaged doping parameters derived from the device simulator. The simulation results are shown in Fig. 6, which shows the NPN Gummel plot comparison between TCAD and SPICE including the common-base current gain parameter α_F. Both simulations show how the parasitic lateral NPN currents and electrical parameter α_F depend on the distance W_b between the two n-wells. Moreover SPICE simulations give accurate and reliable results on parasitic currents reducing simulation time considerably with respect to TCAD (See Table III).

V. Conclusions

Substrate modeling approach with dedicated extraction tool to model lateral parasitic bipolar effects has been presented. Extraction of electrical substrate network is done in seconds for two different wells spacing. Constructed meshing networks of substrate in 3D are illustrated in this paper. The lateral NPN transistor was simulated by SPICE and TCAD. In this example, the simulation time was reduced by approximately 1440 times with respect to the TCAD. The accuracy has been proved by comparison between device and SPICE simulation with an acceptable relevant error. We conclude that SPICE model has a strong advantage in the simulation time.

VI. Acknowledgement

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