HAL
open science

A CAD integrated solution of substrate modeling for industrial IC design

Hao Zou, Yasser Moursy, Ramy Iskander, Jean-Paul Chaput, Marie-Minerve Louërat, Camillo Stefanucci, Pietro Buccella, Maher Kayal, Jean-Michel Sallese, Thomas Gneiting, et al.

To cite this version:

Hao Zou, Yasser Moursy, Ramy Iskander, Jean-Paul Chaput, Marie-Minerve Louërat, et al.. A CAD integrated solution of substrate modeling for industrial IC design. 2015 20th International Mixed-Signal Testing Workshop (IMSTW), Jun 2015, Paris, France. 10.1109/IMS3TW.2015.7177885 . hal-01230118

HAL Id: hal-01230118

https://hal.sorbonne-universite.fr/hal-01230118

Submitted on 17 Nov 2015

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

A CAD Integrated Solution of Substrate Modeling for Industrial IC Design

Hao Zou*, Yasser Moursy*, Ramy Iskander*, Jean-Paul Chaput* and Marie-Minerve Louerat*
Camillo Stefanucci†, Pietro Buccela†, Maher Kayal† and Jean-Michel Sallese†
Thomas Gneiting‡ and Heidrun Alius‡
Alexander Steinmair§ and Ehrenfried Seebacher§
*Sorbonne Universités UPMC Paris 6, CNRS, LIP6 UMR 7606, 4 Place Jussieu 75005 Paris
†Swiss Federal Institute of Technology (EPFL), Laussanne, Switzerland CH-1015
‡AdMOS GmbH Advanced Modeling Solutions, In den Gernaeckern 8, 72636 Frickenhausen
§ams AG, Unterpremstatten, Austria

Email: hao.zou@lip6.fr

***Abstract*—Smart Power IC integrating high voltage devices with low voltage control blocks becomes more and more popular in automotive industry recently. Minority carriers injected into the substrate during switching of high power stages cause malfunction of sensitive nearby low voltage devices. Sometimes this may be destructive due to the presence of triggered latch up. The minority carriers propagation is extremely hard to model and difficult to predict using existing commercial standard design flow. In this paper, we propose a Computer-Aided-Design solution to characterise the substrate vertical and lateral parasitic for Smart Power IC in automotive applications. Investigation of complex benchmark structures is presented. SPICE simulations are performed for extracted 3D substrate netlist and compared to measurements. Good fitting between simulation and measurement validates the effectiveness and accuracy of the proposed CAD tool.**

I. Introduction

Automotive applications requires more and more integration of high voltage (HV) power devices together with low voltage (LV) power control blocks. This integration on a single substrate leads to the development of a new category of integrated circuit (IC), the Smart Power IC [1].

In a typical Smart Power IC, the power switch, the control logic and sensor circuits operate at different voltage levels and temperatures. In such devices, induced substrate coupling noise becomes a critical issue due to switching of the power stages. During switching, parasitic substrate currents consisting of electrons and holes lead to a local shift of the substrate potential that can reach hundreds of millivolts. This is due to the typical presence of inductive loads which can cause forward/reverse biasing of diode junctions during switching with consequent triggering of parasitic bipolar junction transistor (BJTs). As a result, current paths driven by propagation of electrons and holes in the substrate are collected by nearby sensitive analog and digital devices, even at long distance. Minority carriers injected into the substrate during switching of high power stages cause malfunction of sensitive nearby low voltage devices. Sometimes this may be destructive due to the presence of triggered latch up.

Standard industrial design flows do not take into account the minority carriers propagation in the substrate which is hard to model [2]. Technology Computer-Aided-Design (TCAD) tools [3] are considered as a powerful software to model the parasitic substrate coupling effect. However, TCAD applies finite-element method to numerically solve physical equations for 2D and 3D structures. This is usually time-consuming depending on the complexity of layout structures.

In the context of FP7 european AUTOMICS project [4], a Computer-Aided-Design (CAD) tool is developed in order to predict the vertical and lateral parasitic substrate coupling for the industrial automotive applications. This is done by performing SPICE simulations rather than TCAD simulations.

The paper is organized as follows, in Section II a description of complex benchmark structure from ams AG is presented. In Section III EPFL devices used to model the substrate are introduced. In Section IV, parasitic substrate netlist extraction using 3D extraction methodology is described. In Section V, parameter extraction and model calibration process from AdMOS are discussed. Comparison between SPICE simulation of extracted substrate and measurements are shown in Section VI. Finally conclusion is drawn in Section VII.

II. Industrial Complex benchmark structure

Benchmark structure SUBCURR1 is one of the five structures of test-chip designed by ams AG. In this paper, we discuss and focus on the test structure that consists of five identical square n-wells inside P-substrate (diode). Each n-well area is $20\mu m$ times $20\mu m$ as shown in Figure 1. The four leftmost n-well squares are not equally distant from fifth n-well. For this test, the fifth n-well is considered as the emitter. Each of the other wells is considered as the collector for the lateral NPN BJT. Collector currents vary depending on the ditance between emitting and collecting points.

III. Compact substrate model

Compact substrate model has been proposed in order to take into account the minority carriers propagation in circuit

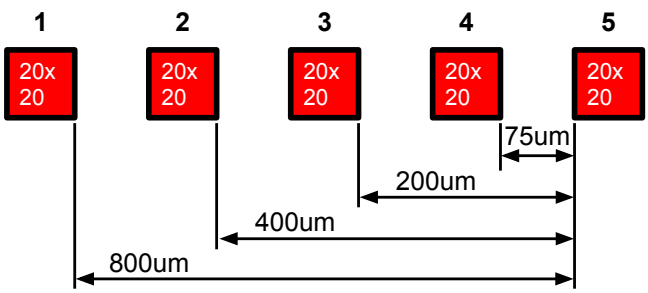


Fig. 1: Benchmark structure SUBCURR1: 5 n-wells connected to PADs 1 to 5 with different distances to fifth n-well

simulation [5]. The substrate model consists of special EPFL devices called *EPFL diode*, *EPFL resistor* and *EPFL homo-junction*. An enhanced contact model for homo-junction has been developed to model the discontinuity between P/P+ and N/N+ homo-junctions [6]. The accuracy of the compact parasitic substrate model depends on the number of instantiated lumped elements in the extracted 3D substrate network. More lumped elements increase simulation time but remains significantly faster than TCAD simulation [7].

IV. Parasitic Substrate Extraction

Within FP7 european project AUTOMICS, the goal is to develop the CAD framework which provides an automatic way to extract the substrate parasitic [8]. The proposed CAD is suitable for extracting industrial chip. Advanced meshing strategies are developed that produce optimised three dimensional mesh network. The idea is to focus on sensitive area in order to extract the minimum number of lumped elements which are:

- DN-PS (Deep N-well to P-substrate) diode
- DN resistor
- PS resistor
- N/N+ homo-junction contact
- P/P+ homo-junction contact

To perform the extraction, we have defined a new extraction rule file including dedicated technology dependent rules, describing the layout cross-section inside the substrate. This file includes also designer selected rules: e.g. select a region to be extracted. We first consider the simple case of Figure 2. It illustrates the deep n-well layer over the P-substrate involving the DN-PS diode. As an example, the rule file corresponding to the cross-section shown in Figure 2 is presented in listing 1. The P-substrate is divided into two slices which are separated by deep n-well: *top* one with depth of X1, and *bottom* one with depth of X2 interconnected with PS (p-substrate) resistances.

```
1 <Layers>
2    <substrate depth="X1+X2"/>
3    <layer name="P+" type="PPLUS"/>
4    <layer name="N+" type="NPLUS"/>
5    <layer name="DN" type="N" depth="X1"/>
6 </Layers>
```

Listing 1: Layout cross-section rules

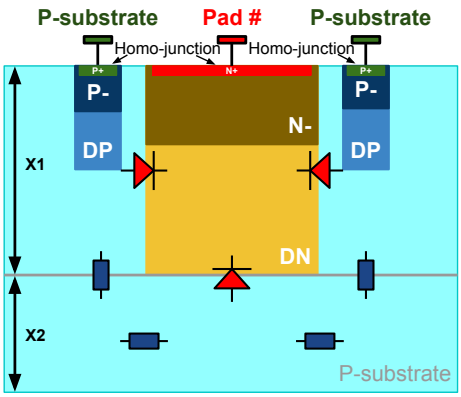


Fig. 2: Layout cross-section view showing one single N-well and the extracted lumped components: DN-PS diode (red), PS resistance (blue), homo-junction contacts (red and green).

Figure 3 represents the resulting layout view and extracted parasitic components of test case (Figure 1) after extraction with the rule file (Listing 1). Only the layers contributing to the extraction of substrate parasitic are presented inside this reduced layout: deep n-wells, highly doped N+ regions and highly doped P+ regions. In this case, DN-PS diode, DN resistance (not shown in figure), PS resistance are extracted from substrate and connected to circuit netlist by homo-junction PPLUS and NPLUS contacts.

The corresponding SPICE netlist is generated by the extraction. It is linked to the EPFL verilog-A model and is ready for simulation and/or back annotation of circuit netlist. It consists of all the extracted substrate parasitic components. Listing 2 shows the typical case of extracted components:

```
1  lang=spectre
2  subckt sub_netlist ( psub_pad1 pad1
3                     + psub_pad2 pad2
4                     + psub_pad3 pad3
5                     + psub_pad4 pad4
6                     + psub_pad5 pad5)
7  // extracted parasitic components
8  I0 (...) smartHomoj_PPLUS (...)
9  I0 (...) smartHomoj_NPLUS (...)
10 I0 (...) smartRes_PS (...)
11 I1 (...) smartRes_DN (...)
12 I3 (...) smartDiode_DNPS (...)
13 ...
n  ends
```

Listing 2: Description of extracted substrate parasitic netlist

V. Model Calibration

Model calibration is a necessary step to determine the values of the model parameters for newly developed substrate parasitic components: EPFL diode, EPFL resistor and EPFL homo-junction contact. In general, such a calibration process could be done as well through TCAD. However, TCAD simulations need a detailed input with respect to doping concentrations and doping profiles, which may not fit the

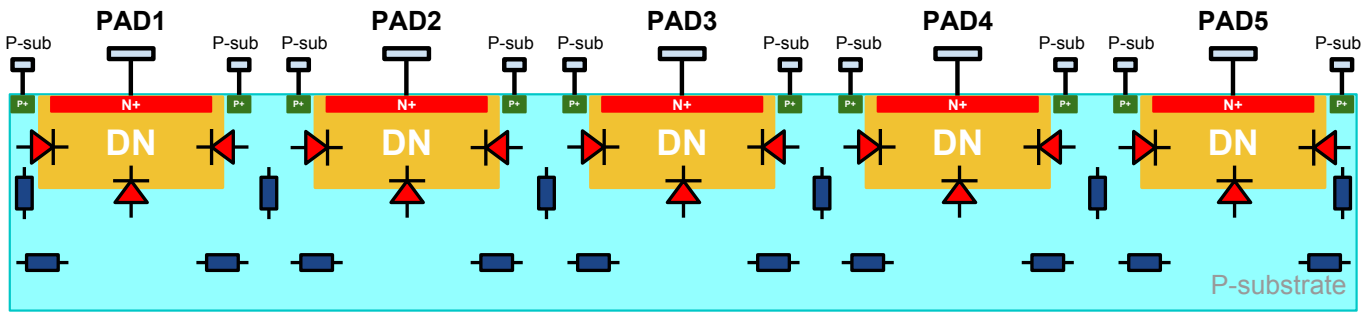


Fig. 3: Reduced layout cross-section view of test case involving five n-wells: deep n-wells, highly doped N+ regions and highly doped P+ regions

actual process conditions used to manufacture a certain well implant. A new strategy for the model parameter extraction is developed by AdMOS. For a dedicated type of well of a certain process, EPFL devices are classified by orientation and doping profiles as illustrated in Figure 4. Therefore, the vertical devices can be differentiated from the lateral ones, allowing to use different values of their model parameters. A control code is added automatically to perform the simulations with the same conditions than in the measurements of the test devices. The simulations are compared to measured data and used by an optimisation algorithm to tune the available model parameters.

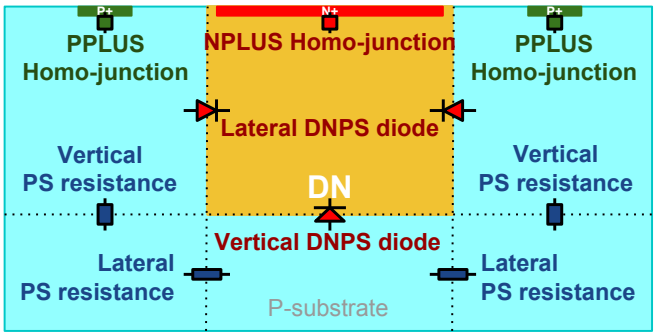


Fig. 4: Different types of EPFL devices for calibration after extracted from tool

VI. Results

The extraction tool provides optimised mesh network in x-y directions which ensures the minimum number of parasitic components to be extracted. Here, we investigate the meshing in z-direction. In this section, several extractions based on the proposed meshing are discussed and their simulations are compared regarding accuracy and effectiveness.

A. Slices extraction strategies in z direction

In the following, we study three different strategies in the z direction:

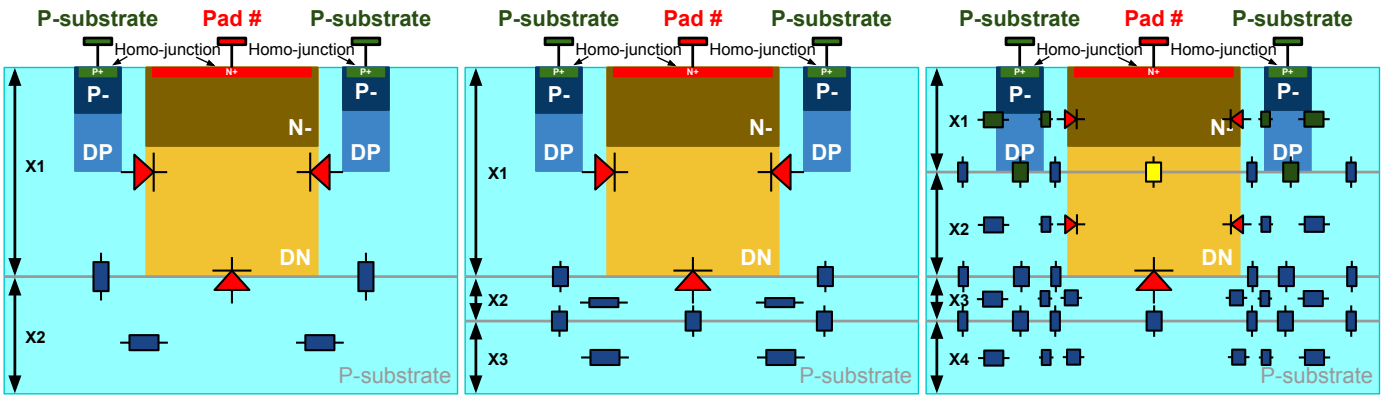
- using two slices: considering only deep n-well over P-substrate as presented in Figure 5a. This is illustrated by case #1 to #4 as shown in Table I.
- using three slices: considering deep n-well and an additional slice in P-substrate as presented in Figure 5b. This is illustrated by case #5 as shown in Table I.
- using four slices: considering deep n-well, deep p-well and an additional slice in P-substrate as presented in Figure 5c. This is illustrated by case #6 as shown in Table I.

Experiments are performed to compare these strategies. Table I summarizes the values used for the extraction and simulation.

TABLE I: List of investigations in z-direction: values *dn* and *dp* are depths of deep n-well and deep p-well in ams technology 0.35μm High Voltage process respectively

#	P-substrate depth (μm)	Nbr. of slices	X1 (μm)	X2 (μm)	X3 (μm)	X4 (μm)
1	22.0	2	*dn*	22-*dn*	-	-
2	50.0	2	*dn*	50-*dn*	-	-
3	100.0	2	*dn*	100-*dn*	-	-
4	200.0	2	*dn*	200-*dn*	-	-
5	200.0	3	*dn*	10	190-*dn*	-
6	200.0	4	*dp*	*dn*-*dp*	10	190-*dn*

Consider first the two slices strategy, as presented in Figure 5a. Four different values of P-substrate thickness are taken into account: 22.0μm, 50.0μm, then 100.0μm and 200.0μm (See table I from case one to four). Since X1 (thickness of Deep n-well) is kept constant, in all cases, then depth X2 is the key parameter of these four different cases. A DC sweep (from -0.2V to -1.2V) analysis is performed, using PAD number five as input, and P-substrate biased at ground. Collected current at PAD number four is monitored by SPICE simulations. Simulation results are compared to measurement in Figure 6. As thickness of P-substrate increases (blue curve to red curve), the simulated collected current decreases, which indeed makes sense since the vertical resistances connecting *top* slice to *bottom* slice increase with the thickness of *bottom* slice. More resistivity causes less diffusion of minority carriers through substrate. In addition, as thickness of P-substrate increases (blue curve to red curve), the accuracy to measurement decreases.



(a) two slices (b) three slices (c) four slices

Fig. 5: Layout cross-section view focus on one single n-well with different strategies of extraction: a) considering only deep n-well, b) considering deep n-well and an additional slice in P-substrate, c) considering deep n-well, deep p-well and an additional slice in P-substrate

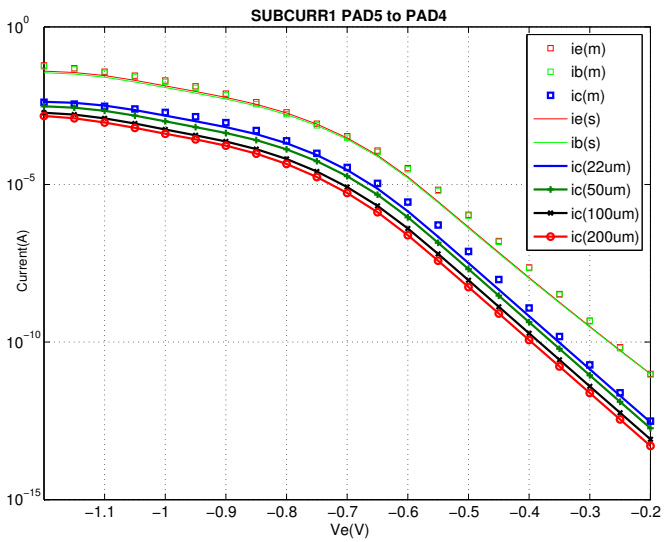


Fig. 6: Substrate netlist SPICE simulations (*"s"*) compared to measurements (*"m"*) of case one to case four: collected currents at PAD four with four different P-substrate depths.

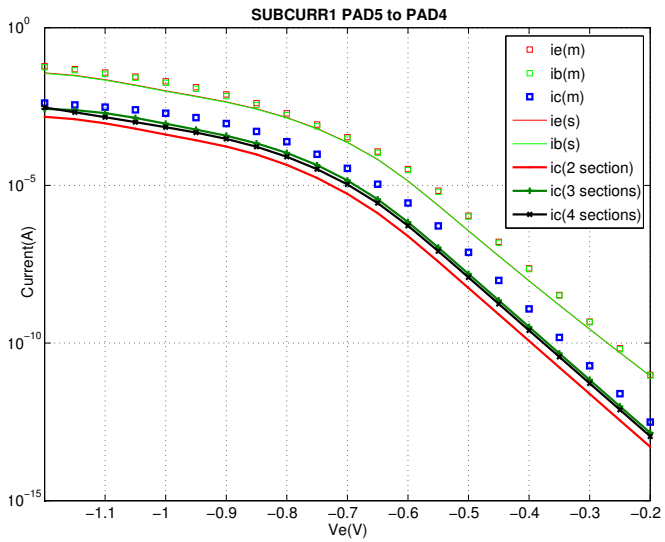


Fig. 7: Substrate netlist SPICE simulation ("s") compared to measurements ("m") of case four to case six: collected currents at PAD four with different meshing in z-direction.

Consider now the three slices strategy, as presented in Figure 5b. It is compared to case number four: the same thickness of P-substrate ($200.0\mu m$) is used, while an additional slice with thickness of $10.0\mu m$ is cut from *bottom* slice. With an additional slice in P-substrate region, a new path for minority carrier diffusion is introduced thus increasing the current collected at PAD number four, which is illustrated in Figure 7 (green curve compare to red curve).

Consider now the four slices strategy, as presented in Figure 5c. We take into account the deep p-well into extraction, thus adding the DP (deep p-well) resistance in substrate parasitic netlist. Green resistance symbol represents DP resistance as shown in Figure 5c, where *top* slice is split into two slices. SPICE simulation results are added in Figure 7 to compare with previous case. Results in Figure 7 show that extraction of deep p-well did not help in this test case to increase the accuracy of extraction. Moreover the case six double the number of extracted parasitic components as presented in Table II.

Comparing case one to six versus measurements, case number five, using three slices strategy is the best one for substrate modeling of this benchmark structure. The accuracy increases by adding an additional slice in P-substrate region close to PN junction.

TABLE II: Report on extraction and simulation (full chip including 5 n-wells)

#	Extraction time (*s*)	Number of nodes (*s*)	Number of elements (*s*)	Simulation time (*s*)
1	2s	1863	2745	14.49
2	2s	1863	2745	32.80
3	2s	1863	2745	21.30
4	2s	1863	2745	34.90
5	3s	2779	4265	22.50
6	5s	4207	6617	845.00

B. Simulation results of SUBCURR1 structure

In this subsection, we use the three slices strategy as presented in previous subsection. We analyze the SUBCURR1 structure by repeating the same experiment for all the PADs of benchmark structure. Emitting current at PAD number five and collecting currents at PAD number one to number four respectively (collecting PAD is biased to ground and others are floating). Figure 8 shows SPICE simulations versus measurements at different collectors (PAD four to PAD one from top to bottom). Results in Figure 8 shows how the parasitic lateral NPN currents behaviour depends on the distance between emitter and collector. Good fitting of SPICE simulation with measurement validates the extracted equivalent substrate netlist, provided by the three slices strategy in different cases.

Dedicated parasitic substrate extraction tool gives a simple and efficient way to model the target industrial benchmark structure in order to investigate substrate coupling behaviours. Accuracy investigations based on slices strategy found out the key parameter to increase extraction accuracy, while keeping simulation time considerably lower than TCAD simulation.

VII. Conclusions

Parasitic substrate modelling solution with integrated Computer-Aided-Design (CAD) framework has been presented in this paper. Industrial benchmark structure was considered as a case study. Focusing on four identical n-well collectors with different spacing to a n-well emitter, enabled to model different lateral NPN bipolar regarding distance variation. Compact parasitic substrate models consisting of EPFL resistor, EPFL diode and EPFL homo-junction contact are used in this work. Model calibration is applied for different devices in substrate models with different geometrical orientation and technological process. The substrate is modeled by a netlist instantiating those different types of devices. Investigations on accuracy of three dimensional netlist identified the key parameter to increase the accuracy in view of extraction. Results showed a good fitting between simulation of extracted netlist and measurement. Accuracy and reliable results validate the extraction tool and shows the usability for automotive industry.

VIII. Acknowledgement

This work was supported by the project AUTOMICS: Pragmatic solution for parasitic-immune design of electronics ICs

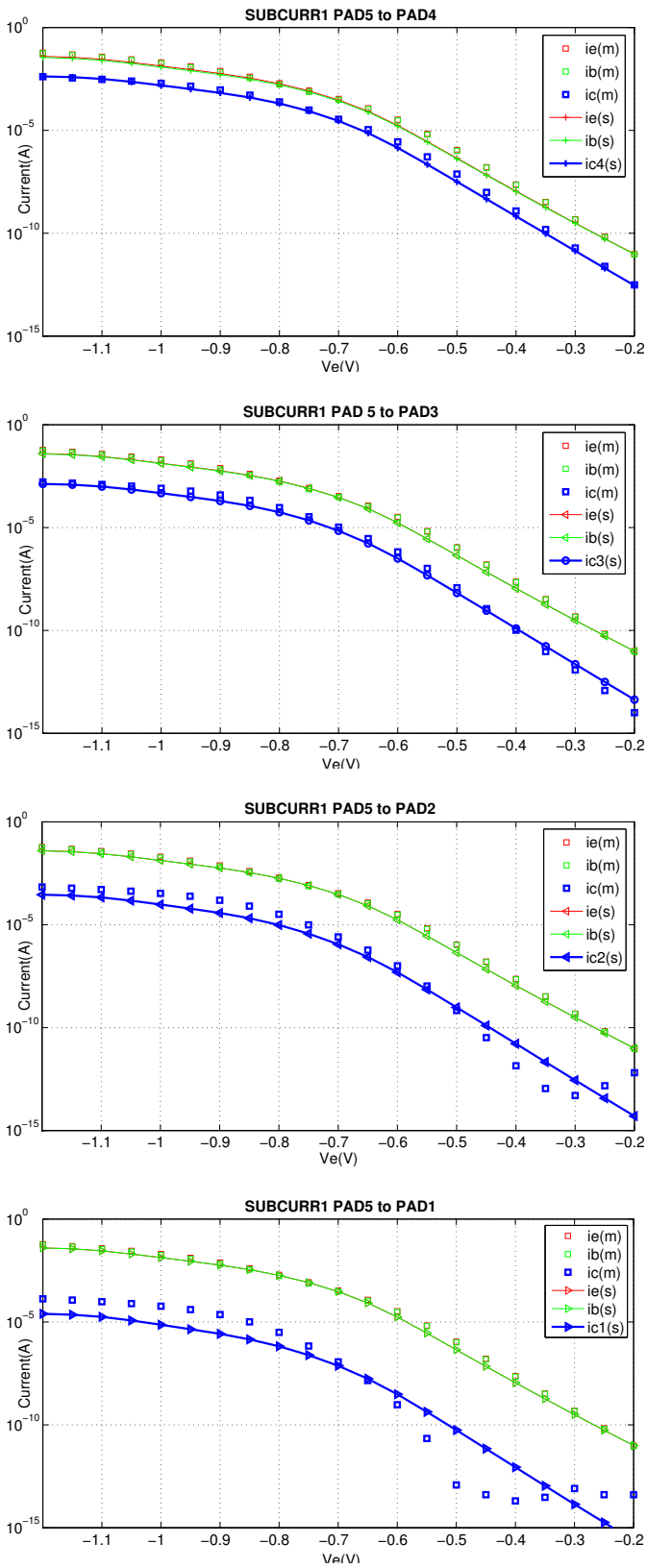


Fig. 8: Substrate netlist SPICE simulations ("s") versus measurement ("m"): diagrams from top to bottom represent collected currents at PAD four, at PAD three, at PAD two and at PAD one respectively.

for automotive, which is funded by the European Commission within the 7th Framework Program (FP7/ICT 314135).

REFERENCES

[1] B. Murari, F. Bertotti, and G.Vignola, *"Smart Power ICs,"* 2nd ed. Berlin, Germany: Springer-Verlag, 2002, pp. 218-220.

[2] F. Lo Conte, J. M. Sallese, M. Pastre, F. Krummenacher, and M. Kayal, "Global Modeling Strategy of Parasitic Coupled Currents Induced by Minority-Carrier Propagation in Semiconductor Substrates", IEEE Trans. Electron Devices, vol. 57, pp. 263-272, January 2010.

[3] Synopsys Sentaurus Device, http://www.synopsys.com/tools/tcad

[4] Y. Moursy et al., *"AUTOMICS: A novel approach for substrate modeling",* 18th IEEE European Test Symposium, May, 2013.

[5] Lo Conte, F.; Sallese, J.-M.; Kayal, M., *"Modeling methodology of high-voltage substrate minority and majority carrier injections,"* Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European , vol., no., pp.194,197, 14-16 Sept. 2010.

[6] Stefanucci, C.; Buccella, P.; Kayal, M.; Sallese, J.M., *"Impact of enhanced contact doping on minority carriers diffusion currents,"* Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in , vol., no., pp.1,4, June 30 2014-July 3 2014.

[7] Stefanucci, C.; Buccella, P.; Kayal, M.; Sallese, J.M., *"Optimization strategy of numerical simulations applied to EPFL substrate model,"* Mixed Design of Integrated Circuits & Systems (MIXDES), 2014 Proceedings of the 21st International Conference , vol., no., pp.334,337, 19-21 June 2014.

[8] Hao Zou; Moursy, Y.; Iskander, R.; Louerat, M.-M.; Chaput, J.-P., *"A novel CAD framework for substrate modeling"* Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in , vol., no., pp.1,4, June 30 2014-July 3 2014.