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Charge Collection Efficiency in a Segmented Semiconductor Detector Interstrip Region

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Abstract

Charged particle semiconductor detectors have been used in Ion Beam Analysis (IBA) for over four decades without great changes in either design or fabrication. However one area where improvement is desirable would be to increase the detector solid angle so as to improve spectrum statistics for a given incident beam fluence. This would allow the use of very low fluences opening the way, for example, to increase the time resolution in real-time RBS or for analysis of materials that are highly sensitive to beam damage. In order to achieve this goal without incurring the costs of degraded resolution due to kinematic broadening or large detector capacitance, a single-chip segmented detector (SEGDET) was designed and built within the SPIRIT EU infrastructure project. In this work we present the Charge Collection Efficiency (*CCE*) in the vicinity between two adjacent segments focusing on the interstrip zone. Microbeam Ion Beam Induced Charge (IBIC) measurements with different ion masses and energies were used to perform X-Y mapping of *CCE*, as a function of detector operating conditions (bias voltage changes, detector housing possibilities and guard ring configuration). We show the *CCE* in the edge region of the active area and have also mapped the charge from the interstrip region, shared between adjacent segments. The results indicate that the electrical extent of the interstrip region is very close to the physical extent of the interstrip and guard ring structure with

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interstrip impacts contributing very little to the complete spectrum. The interstrip contributions to the spectra that do occur, can be substantially reduced by an offline anti-coincidence criterion applied to list mode data, which should also be easy to implement directly in the data acquisition software.

Introduction

The advance of IBA towards studying more complex materials, together with new technical possibilities, are driving factors for the development of IBA detection and data acquisition systems. In particular, the statistics of charged particle detection play a great role in the quantity and quality of information that can be extracted from a given RBS or NRA experiment [1]. Increasing the detector solid angle will allow increased statistics for a given beam fluence, which will enable some limitations to be overcome. These include detection or determination of elements present below the present detection or quantification limit, measurements on materials sensitive to ion beam damage, such as some monocrystals or organic materials [2], [3], and use of very low ion currents, such as doubly charged alphas from a standard RF ion source accelerated to double the beam energy for singly charged ions in a single ended electrostatic accelerator. Increasing the overall detection solid angle must be accomplished whilst maintaining a low kinematic energy spread. A limited detector surface area is also desirable since a large detector surface will generate significant electrical and thermal noise, and under standard analysis conditions the count rate could be very high, leading to significant deadtime and pileup. A segmented detector design – composed of an array of individual detectors of appropriately chosen geometries meets these criteria so long as a suitable number of pulse-shaping and data acquisition channels are also available. A segmented detector will also contribute to resolving the mass-depth ambiguity in RBS since spectra will be collected for several detection angles [4].

In the present work, we have studied Charge Collection Efficiency (*CCE*) of a large solid angle semiconductor segmented strip detector (SEGDET) built in the framework of the SPIRIT EU project at HZDR. The detector is composed of 16 individual segments with a Guard Ring (GR) dividing them. We focus on the charge collection in the interstrip region between two adjacent segments, applying the Ion Beam Induced Charge (IBIC) technique with a scanning ion microprobe. We have investigated how the charge from the interstrip region may be shared between adjacent active zones, as well as the role of the GR, using different incident ions and energies.

Instruments and methodology

The SEGDET used in this work is made by standard semiconductor processing techniques: ion implantation, lithography, thermal oxidation, metal deposition, annealing and so on. As a substrate a (100)-oriented, n-type Si wafer ($N_D \approx 1 \cdot 10^{12} \text{ cm}^{-3}$, $\rho = 5500 \text{ } \Omega\text{cm}$) is used. The implanted donor in the p+ entrance window is B⁺ (10 keV, $N_D = 5 \cdot 10^{14} \text{ cm}^{-2}$) and the acceptor is P⁺ implanted to form the rear n+ contact (50 keV, $N_D = 5 \cdot 10^{14} \text{ cm}^{-2}$). The implantation was made through a SiO₂ layer (60 nm) which was removed after the implantation. Al was deposited to create the ohmic contacts. The structure of two adjacent segments with the interstrip region in between is shown in Figure 1. The complete detector area is $29 \times 29 \text{ mm}^2$, divided into 16 segments ($29 \times 1.79 \text{ mm}^2$), as is shown in Figure 2.a. The microscopic view of the interstrip region is shown in Figure 2.b; where two adjacent segments are the active areas (Segment A and B), SiO₂ is the passivation zone which delimits the segment border, and the central part is the aluminium GR which is intended to isolate the segments – avoiding crosstalk as much as possible, keeping the electric field at the edge under control and reducing the leakage current.

To characterize the detector electronically, the leakage current was measured under different bias and GR configurations. The segment depletion thicknesses were measured via standard C-V curves.

The IBIC technique has been used to study the *CCE* in the last two decades for different semiconductor devices [5], [6]. It consists in the measurement of the charge carriers induced by the incident high energy ion in the depletion region of the p-n junction (Figure 3). IBIC measurements were made at the Ruđer Bošković Institute, using a microprobe of $1 \times 1 \text{ } \mu\text{m}^2$ size and scan lengths from $250 \text{ } \mu\text{m}$ up to $650 \text{ } \mu\text{m}$ in X and Y (Figure 3). The incident ions used were $^1\text{H}^{1+}$ at 4.5 MeV , $^{12}\text{C}^{3+}$ at 5.5 MeV and $^{12}\text{C}^{4+}$ at 6 MeV , where the differences in the charge state for C ions are negligible for the IBIC measurements. The incident ion fluxes were between $10^2 - 10^3 \text{ s}^{-1}$. Two classical analogue charge acquisition channels were used to acquire the induced charge as a function of the X-Y scan position.

For the C ions three different GR configuration were used: GR biased at the same potential as the segments, GR not biased and GR floating.

Results and discussion

The main subject of this study is the role of the GR in the SEGDET, therefore the first stage is to measure the electronic response without beam. The leakage current through both segments and the GR was measured and plotted as a function of GR bias as is shown in Figure 4. Note that the 'no bias' configuration is when the power supply plug in the GR is switch off, but nevertheless a parasitic voltage due to the adjacent segment electric field appears in the display (when the segment voltage is -80 V , for example, the GR voltage is -10.9 V). In the graph it can be seen that almost no leakage current has been found in the segments when the GR is biased, no matter which voltage is implemented, however the current is great when there is no bias on the GR. When GR is floating we are in an intermediate case. Since the energy resolution depends on the leakage current [4], the optimal configuration so far is biasing the GR.

Figure 5 shows the C-V curve and the p-n junction depletion thickness as functions of segment bias. The maximum depletion thickness of $260\text{ }\mu\text{m}$ is reached at -100 V applied bias. For the main bias voltages -20 V , -30 V , -80 V used in the later IBIC experiments the depletion thicknesses are $162\text{ }\mu\text{m}$, $192\text{ }\mu\text{m}$, $255\text{ }\mu\text{m}$, respectively. Note, that at 0 V segment bias there is an intrinsic depletion thickness of $32\text{ }\mu\text{m}$.

IBIC measurements were normalised by taking the charge collection efficiency (CCE) within the segments (detector active zone) as equal to 1 at the highest bias voltage (-80 V), neglecting the energy loss in the dead layer ($\sim 100\text{ nm}$). Figure 6 shows the variation of *CCE* in the segments with respect to the applied bias voltage when a ${}^1\text{H}^+$ 4.5 MeV beam is used. The ion range in silicon given by SRIM [7] in this case is $180\text{ }\mu\text{m}$. We note that *CCE* reaches the maximum at a bias of -20 V , which corresponds to a depletion region of $162\text{ }\mu\text{m}$ as measured above. This is 10% less than the proton range, however with the tile constants of the preamplifier and pulse shaping amplifier used here the

charge induced beyond the depletion zone can still be collected. The two adjacent segments showed identical behaviour.

The *CCE* behaviour in the interstrip region has been studied by extracting a line scan across the interstrip region from the 3D IBIC map to represent a 2D graph with the average *CCE* values projected onto the Y axis, as is shown in Figure 7 for $^1\text{H}^+$ incident ions at 4.5 MeV and in this case keeping the GR floating and segment bias at -30 V. Three zones can be identified: A) Detector segment, where $CCE = 1$, B) SiO_2 passivation, in which the *CCE* is slowly decreasing, and C) GR, where the *CCE* drops drastically and the signal is present in both acquisition channels. The number of events present simultaneously in both acquisition channels was calculated using an off line coincidence data treatment, and showed that the induced charge is shared (i.e. adjacent segments cross talk). The coincident events decrease with the bias from $5 \cdot 10^{-2}$ to $2.4 \cdot 10^{-2}$ % coincidences/ μm^2 ; therefore, taking into account that the active detector area is in the order of $10^5 - 10^6 \mu\text{m}^2$, these events are negligible.

To define the different zones within the interstrip region more clearly it is desirable to use a heavier incident ion since it increases the *CCE* contrast in the X-Y maps [8]. Here we used $^{12}\text{C}^{3+}$ and $^{12}\text{C}^{4+}$ ions, both equivalent in the point of view of induced charge at 5.5 MeV for $^{12}\text{C}^{3+}$ and 6 MeV for $^{12}\text{C}^{4+}$. SRIM gives ion ranges in silicon of 5.42 μm and 5.86 μm , respectively. Using the same line scan averaging as above, Figure 8 shows the *CCE* for the three different GR configuration when the segments are biased at -30 V. When the GR is biased bias (black line), the edge of the electric field in both segments is well defined, and the crosstalk has been eliminated. However the *CCE* within the segments is 15% lower. On the other hand both the floating (blue line) and the no bias (red line) GR configurations represent a $CCE > 1$ in the interstrip region and surroundings. This might be explained by the highly charged states of the C ions and high charge density along the ion tracks which this set up involves, where either light generation in the SiO_2 or electron cascades could generate extra charge inside the detector interstrip resulting in a $CCE > 1$. To characterize this behaviour further studies using *CCE* simulations

and systematic experiments with different device configurations are needed. Nevertheless, these heavy ions in those last GR configuration are giving us more information about the interstrip structure. When the GR is not biased, the CCE vs Y graph is mostly symmetric, where the $CCE > 1$ is extending around 15 – 20 μm into the detector segment; then CCE is stable in the Al contact region, increasing up to 1.6 in the SiO_2 passivated zone. Approximately in the central part of the SiO_2 the CCE starts to drop dramatically until the zone below the GR is reached. The charge is shared from the SiO_2 edge, however the number of these coincident events is very low, around $3 \cdot 10^{-4}$ % coincidences/ μm^2 . The floating GR case is more asymmetric since there is no reference for the generated electric field. Nonetheless, a CCE peak can be seen in the Al contact edge between regions A and B, rather than the smooth drop observed in the no bias case. Here the number of shared events is even smaller, around $1 \cdot 10^{-4}$ % coincidences/ μm^2 .

Conclusions

The role of GR for our SEGDET has been clarified for the correct installation and routine use. We have shown that GR biased with the same voltage as the segment reduces the leakage current significantly, hence electrical and thermal noise contribution for the energy resolution is also reduced. For $^1H^{1+}$ ions, the CCE variation with applied bias seems to be in good agreement with the C-V measurements.

The charge generated in the interstrip region may be shared by two adjacent segments, however the number of these events is very small and can be either treated by anticoincidence methods or even neglected. Nevertheless biasing the GR further reduces this charge sharing, and therefore, there is no need for any external segment shield (such as a strip mask in front of the detector interstrip regions) to avoid crosstalk between the segments.

The $CCE > 1$ generated by the ^{12}C ions in the interstrip region cannot be unequivocally explained with the present experimental results. Detailed electric field calculations and device simulations may shed further light on these observations.

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Figure 1

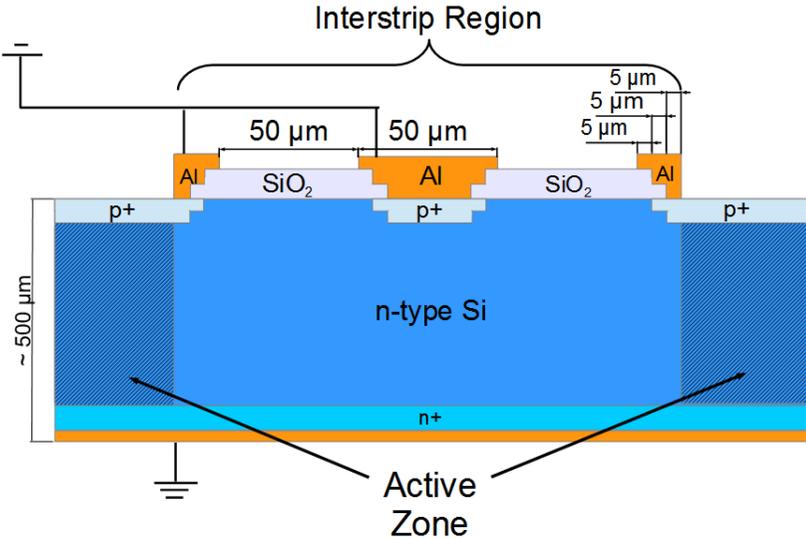


Figure 2

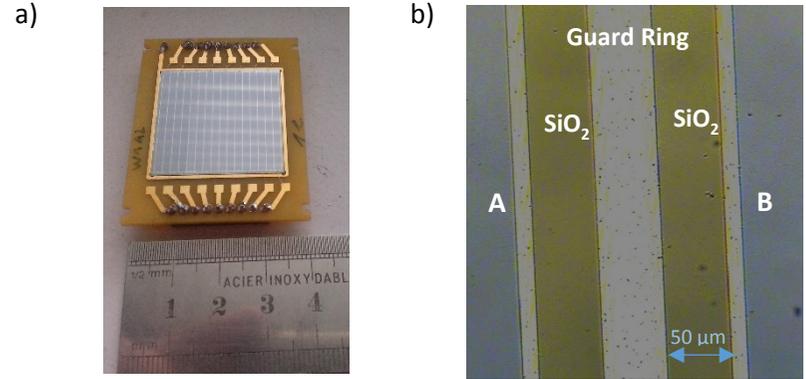
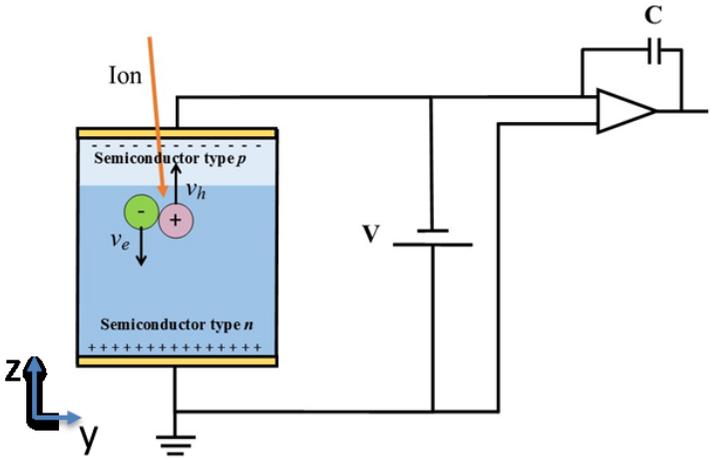


Figure 3

a)



b)

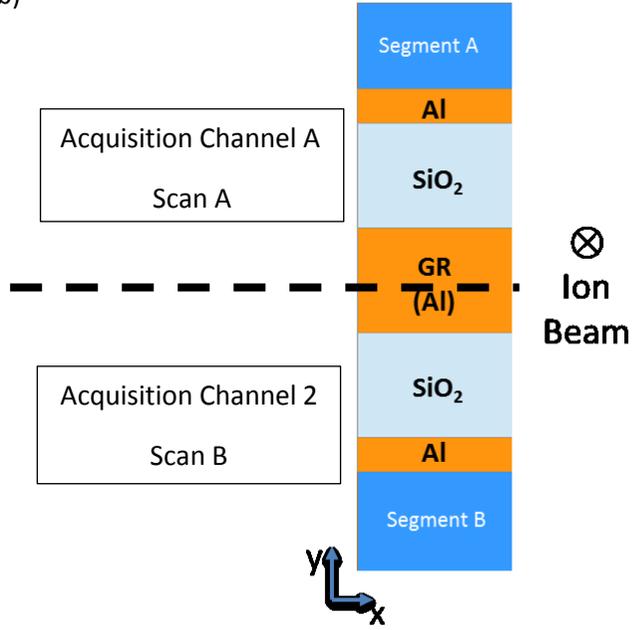


Figure 4

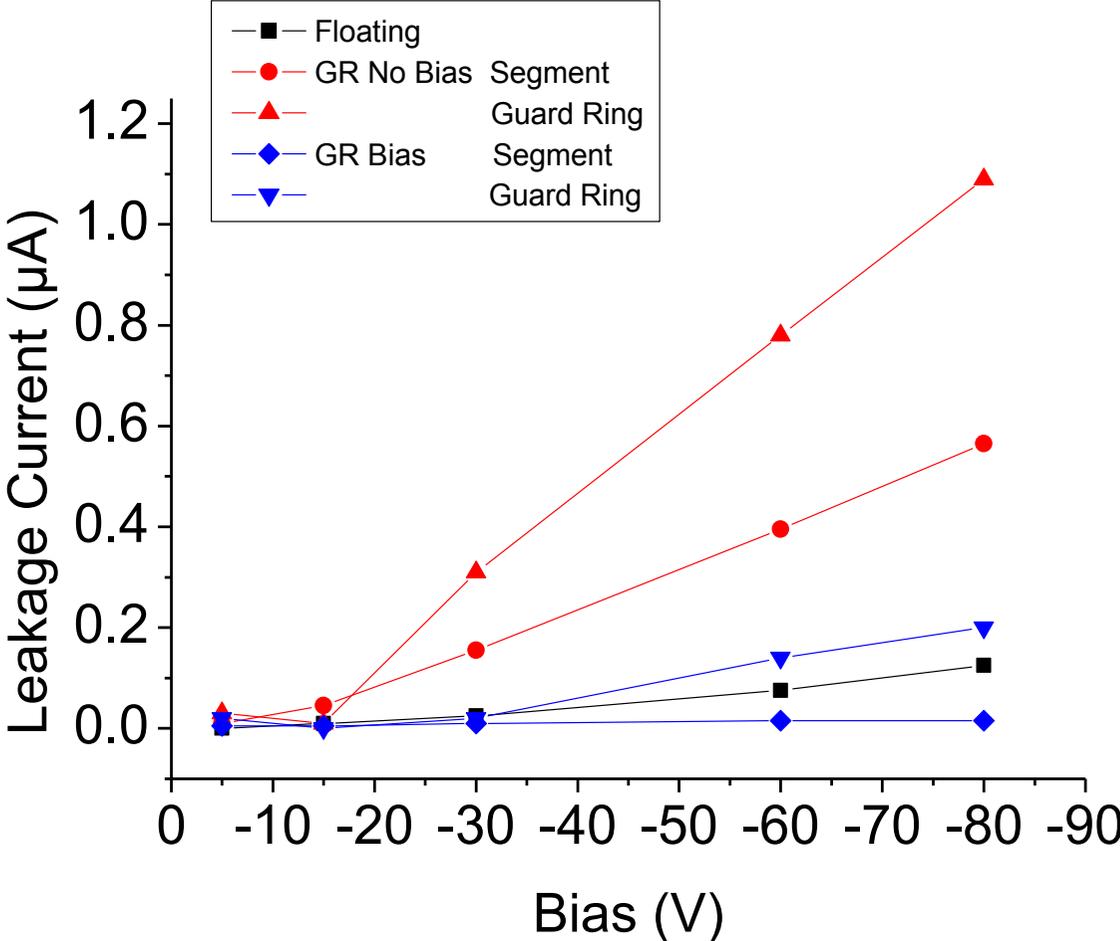


Figure 5

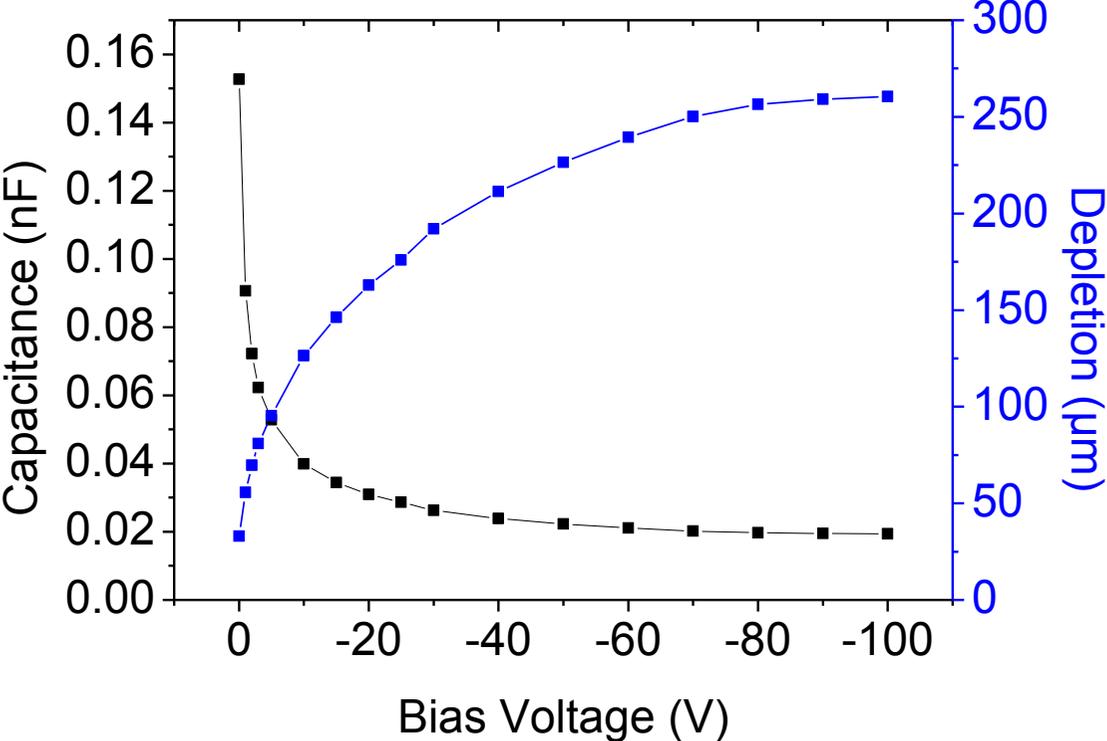


Figure 6

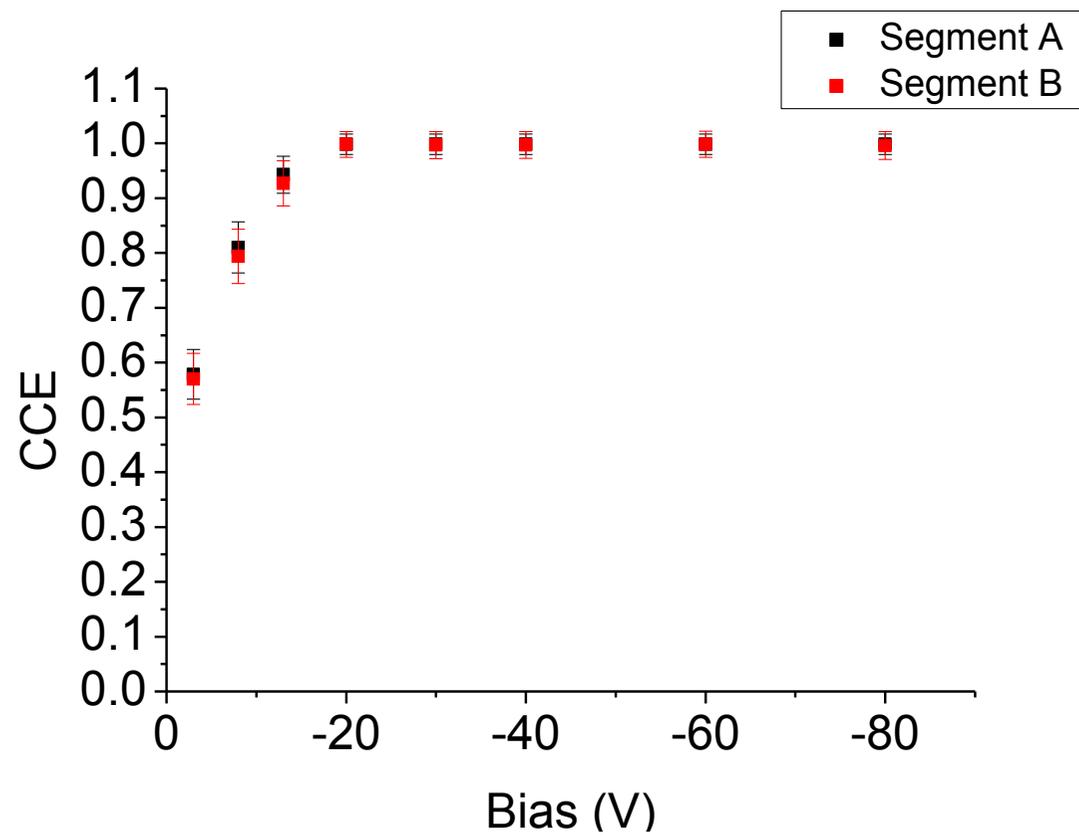


Figure 7

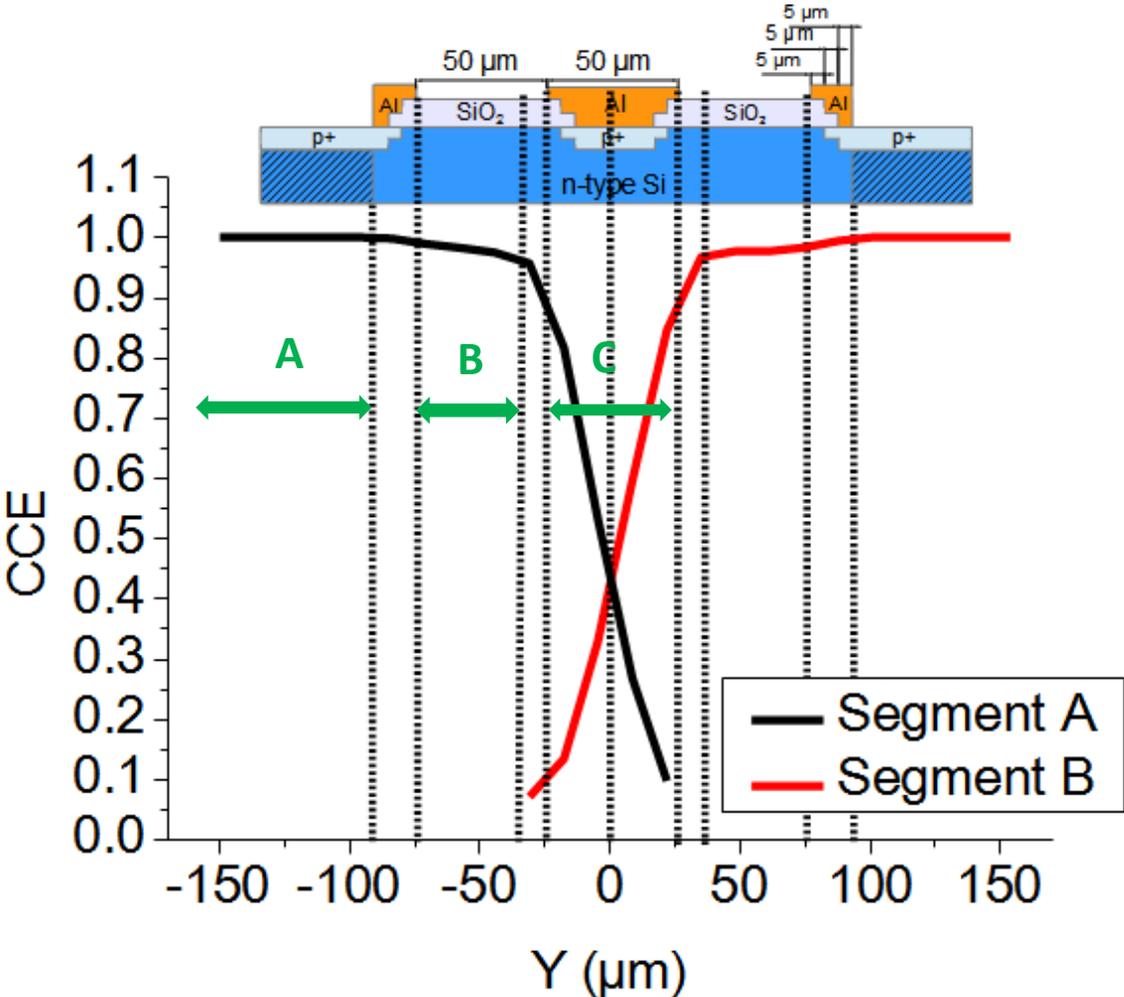


Figure 8

