Highly configurable place and route for analog and mixed-signal circuits

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***Abstract*—Analog design remains a manual task because of the complexity of the interations among devices. Automation tools dedicated to analog circuits are not as mature as the digital automation tool but have been improved a lot, at a point that they can help at individual steps in the analog design flow. This Ph. D. thesis is oriented toward creating a semi-automated mixed design flow controlled by the designer with a particular focus on an analog and mixed signal placer and router. The results show the ability of our tool at generating multiple placed and routed layouts respecting designer's constraints.**

I. Context and motivations

An automatic place and route tool should produce analog device-level layouts similar in density and performance to the high-quality manual layouts. To achieve this task, the capability to deal with layout constraints, in order to decrease unwanted parasitics due to the process variations, is mandatory [1].

Recent research focused on using simulated annealing algorithm [2] in combination with topological representations to respect these analog constraints. Topological representations encode the positioning relations between devices and the optimizer alters their relative positions. The most popular representations are Sequence-Pair [3], B*-Tree [4], Transitive Closure Graph [5], Ordered-Tree [6] and slicing floorplans [7] and they are coupled with some constraints to respect at the same time.

Although most of the recent works focus on highly automated approaches based on optimization processes [8], we believe that giving more control to designers and using their interventions to set some constraints is mandatory to get resulting layouts accepted by designers. Our semi-automatic approach also helps designers to debug more efficiently and makes adjustments easier while some tiresome and error-prone tasks are automated.

II. Analog Placement

Digital and analog circuits have a dedicated area on a system-on-chip circuit so they can be independently designed within a specific space (fig. 1). It is also common to design analog circuit in rows of devices where the height of each row of devices should be adjustable so it can match its dedicated area. In order to organize devices in row, we use the slicing tree structure which will be specified by designers. Having designers defining the slicing tree, it means they will have control over the global topological placement. Their choice will impact on analog placement constraints such as promixity range, signal path and regularity.

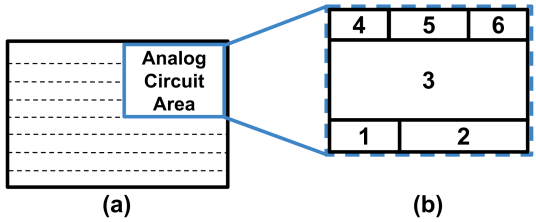

Fig. 1. Mixed signal circuit floorplanning and analog placement in 3 rows

To set rows of devices, the height of each device needs to be similar and to do so, designers have to consider possible aspect ratios for each device by varying their number of fingers. In a bottom-up propagation manner, designers will have choices of multiple placements' results ordered according to their total aspect ratio. Designers also have control over margin tolerances which can eliminate some placements if devices' height in a row are too different.

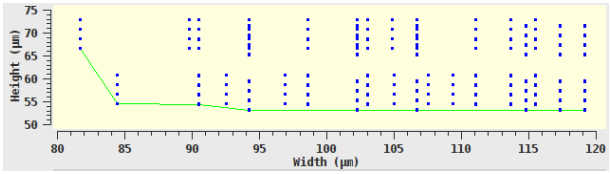

Fig. 2. Circuits possible dimensions graph

Once designers define their slicing tree and the previously mentioned constraints, our placer will process the accepted placements in a few seconds and present them on an interactive graph (fig. 2). Each point of the graph represents a valid placement and its coordinates are its width and height. A point can be selected and our placer will generate, in less than a second, the according placement. Designers can pick the most appropriate placement based on his experiences and the aspect ratio of the floorplan.

III. Analog and Mixed Signal Routing

Once the placement phase is performed with the slicing tree, it is then used for the routing phase. The purpose of this work is to place and route mixed signal circuits, this is the reason why our router has been built through a common

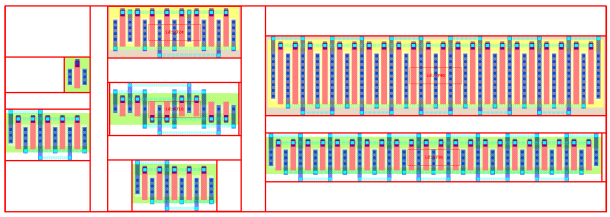

Fig. 3. Global routing structure used for the Dijkstra algorithm

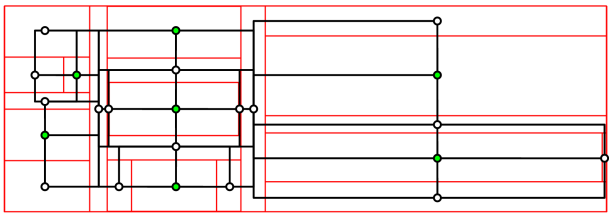

Fig. 4. Graph of relation between devices and routing channel used for the Dijkstra algorithm. Green nodes are devices and others are routing channels.

design flow for routing digital and analog parts. It is divided into two steps: a global routing step and a detailed routing step.

1) Global Routing: To iniate the global routing step, the slicing tree used for the placement is going to be converted into a graph of relation between rectangular areas (fig. 3&4). Each area represents either a device or a channel where wire will be routed. The goal is to establish by which areas each wire is going to pass by. The search of the shortest paths is performed using the Dijkstra algorithm because it is easy to configure constraints. Designers can set restrictions concerning devices which must avoid routing over themselves. Designers can also set routing constraints such as symmetry, wirelength and topology constraints for some specific signal paths that require special attention. Based on the routing estimation, routing channel are then enlarged in order to leave enough space for wires to be placed by the detailed routing phase.

2) Detailed Routing: The goal of detailed routing is to assign route segments of signal nets to specific routing tracks, vias, and metal layers with given global routes of those nets. The detailed router works as a channel router manner. Each cut of the slicing tree is considered as a routing channel that can be expanded based on a routing estimation leaving enough space for wires. Constraints specified by designers need to be respected in this step. Routing channel is performed by respecting symmetric nets, topology-matching constraints and wirelength constraints.

IV. Results

Our tool was implemented in C++ programming language on a Intel(R) Core(TM) i5-4590S CPU @ 3.00 GHz workstation with 6 GB RAM. To illustrate the capability of our tool, we experiment it on a fully differential transconductor [10], designed in 130nm CMOS technology process (fig. 5).

The fully differential transconductor is composed of a total of 32 devices and we consider 2 possible variations for each device. The slicing tree takes into account 11 symmetries

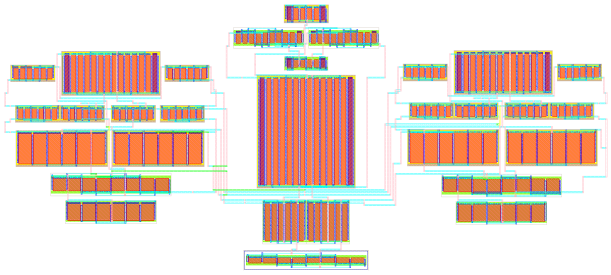

Fig. 5. Placed and routed fully differential transconductor [10] in 130nm CMOS technology process

for this circuit and tolerance margins are set in a way to have reasonnable amount of accepted possibilities. Designers can choose their final placement based on their experiences and preferences. After choosing a placement, we perform the routing step that is performed in less than 5 seconds to obtain the results on fig. 5. In case the final result does not satisfy designers, they can try another placement to be routed easily and in matters of seconds.

V. Conclusion

This Ph. D. thesis is about creating a highly configurable analog and mixed signal placer and router. Placement is realized using the slicing tree as floorplan representation to organize circuits in rows of devices for regularity. Designers choose their desire placement among multiple placement results that can be selected and generated in a few seconds. Their choice is based on their experience and the aspect ratio of the placement. The mixed signal router is able to handle digital and analog router through a common software structure. Analog circuits are routed with particular constraints such as symmetries, topology and wirelength constraints.

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