Open Source Hardware and EDA Tools for Analog/Mixed-Signal Design and Prototyping

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***Abstract*—The paper aims at stimulating a discussion on the prospect and potentiality of open source electronic design automation tools and open source hardware. We discuss the benefits and motivation, as well as the expected difficulties and shortcomings. Finally, we provide a representative list of efforts as of today specifically for analog and mixed-signal circuits and systems design and prototyping.**

I. Introduction

Electronic Design Automation (EDA) tools aiming to perform modeling, design, simulation, verification, design-for-test, etc., of electronic circuits and systems are commercialized and, thereby, "un-democratized", in the sense that licenses come at a price that is prohibitive for individuals and in many cases for Universities and small and medium size enterprises as well. Even if access to EDA tools is granted, the subsequent circuit fabrication and hardware prototyping steps are also very costly and cannot be easily afforded either.

In light of this reality, as of today there have been many attempts towards open source EDA tools (OSEDA) and open source hardware (OSHW), turning electronic circuits and systems design from being a "privilege" to being accessible at a personal scale [1]. Open source in this context means that the source code of EDA tools and netlist, layout, benchmark suites, etc., of a hardware design, are made publicly available and are freely distributed with no discrimination against persons or groups, and, thereby, they can not only be used freely, but can also be modified and enhanced with new features for the specific needs of a project [2]. Furthermore, a first version of OSEDA or OSHW can continuously evolve through the work of additional, multiple, and independent contributors in a collaborative spirit.

OSEDA can be considered as part of the free open software movement [3] and OSHW can be considered as part of the worldwide makers movement or a technology-based extension of the Do-It-Yourself (DIY) movement [4], [5].

One of the first pioneers of OSEDA was University of California, Berkeley, proposing a variety of tools for circuit design [7]. Perhaps the most popular OSHW nowadays is Arduino [8], which offers the possibility of fast hardware prototyping without requiring the user to have a strong background in electronics and programming. Historically, OSEDA and OSHW have been developed more intensively for digital circuits compared to their analog counterparts [5]. For example, Alliance [9], [10], which is a tool for digital integrated circuit design allowing the automated synthesis of a circuit from Registered Transfer Level (RTL) description to Graphic Database System (GDSII) description, was proposed in the early 90s. An excellent and comprehensive review of OSEDA and OSHW efforts, as well as existing project repositories (for example, see [11]–[13]), can be found in [14]. The ongoing project "Open!" is studying the current practices in open source project development [6].

In this paper, we provide some representative examples of existing and under development OSEDA and OSHW specifically for analog and mixed-signal (AMS) circuit design and prototyping. Due to space limitations the list is not meant to be complete. Section II discusses the benefits from widely adopting OSEDA and OSHW which explains the growing interest of the designers community. Section III discusses the difficulties for OSEDA and OSHW to become a reality and common practice. Section IV provides the examples and Section V concludes the paper.

II. Motivation for OSHW and OSEDA

OSHW and OSEDA will greatly increase the number of individuals (i.e. makers, passionates of electronics, curious, etc.) who can perform designs. It will also allow small and medium size enterprises that do not necessarily have the capital to purchase licenses of proprietary tools and hardware platforms to perform designs. The larger pool of designers created by OSHW and OSEDA implies that innovation will be brought up at a faster pace. There will be more innovation and higher productivity through reuse especially on what it concerns application-specific integrated circuits, thus allowing the development of new products and applications. As a result, OSHW and OSEDA can facilitate the proliferation of electronic circuits, extending their deployment in a broader range of applications.

OSHW and OSEDA will be valuable for supporting teaching activities on electronics at Universities even in countries and continents that have limited financial means. Students anywhere in the world will be able to put their hands on actual designs, learn, experiment, and even make silicon demonstrators. OSHW and OSEDA can be used even in secondary education such that students get exposure to electronic design and design automation at a very early stage.

OSEDA will bring down drastically the cost of designing an integrated circuit. This not only reduces the final product cost, but also allows the design companies to invest the amount that would be spent otherwise to purchase licenses of proprietary tools for other purposes, such as performing more design iterations, fabricating more prototypes, and adding more features into the design that often are overlooked due to cost factors, i.e. built-in test infrastructure, security, reliability, self-repair, fault tolerance, etc.

Since the number of designers increases and the cost of design drops, there will be more designs that reach a silicon implementation, thus overall there will be more clients for the foundries. Apart from the economic benefit, this will sustain a high volume manufacturing of devices in a current technology for a longer period. Therefore, the investment on a foundry, which is typically in the order of tens of billions of U.S. dollars, will amortize itself faster and, in general, the phenomenon of rapid technology obsolesce will slow down. In addition, we may observe the sustainability of foundries in several countries, thus partially alleviating security and trust concerns, such as IC/IP piracy, counterfeiting, overproduction, etc., that are due to outsourcing and the globalization of the manufacturing chain of electronic components.

OSEDA may motivate or even force in the end foundries to freely distribute their process design kits (PDK). This will circumvent complications that designers often experience with the signing of the Non Disclosure Agreement (NDA). For example, often in the case of academic projects the foundry demands the ownership of the design.

OSHW and OSEDA will also facilitate the creation of benchmark circuits that can be used for demonstrating and comparing concepts. It is often the case that for a given problem numerous solutions are proposed in the literature, but it is impossible to perform a quantitative comparison because the underlying case studies in each paper, i.e. circuit, topology, technology, etc., are different. Benchmarks can help evaluating and comparing solutions on common grounds, thus offering more credibility to published papers and avoiding the flood of literature. Benchmarks can help also practitioners selecting much faster the best solution for a given application.

EDA companies tend to decompose the tool for performing and completing successfully a design into several individual tools, each requiring a different license. OSEDA could target an all-in-one tool or combine OSEDA tools with licensed tools.

Using proprietary tools for which the source code is not available introduces various trustworthiness and security threats. In particular, there are various vulnerable points that can be exploited by a knowledgeable adversary to introduce Hardware Trojans. Hardware Trojans are malicious modifications in an IC aiming at covertly leaking secret information, such as cipher keys in a cryptoprocessor, degrading the reliability and performance, rendering the IC completely malfunctional, or bringing the IC at a denial of service state. OSEDA can offer full transparency for the user who, in turn, will have full control over the design. Assuming a chip designed entirely with OSEDA and a trusted foundry, the Hardware Trojans threat is eradicated.

It is commonly accepted that the benefits from OSHW would be greater if it is supported by publicly available documentation regarding the EDA tools that were employed to develop the OSHW [15]. OSEDA is a key factor to reach this goal.

OSHW and OSEDA are based on the principle that anyone can be a user of a released version and a contributor in a future version. The different versions can also be traced back to understand the evolution. In this regards, OSHW and OSEDA become automatically world heritage that is by default preserved indefinitely and can further evolve at any chosen time even after a long period of silence [16].

III. Difficulties and challenges for OSHW & OSEDA to become reality

If a large number of chip designers start relying on OSEDA, then EDA companies will face financial losses and this may bring them out of business resulting in significant job cuts. A new business model will be needed, perhaps a support-oriented business model. Nevertheless, as explained above, OSEDA are expected also to create jobs and even new markets, thus the job cuts in the EDA industry may be counterbalanced.

Continuous and quick maintenance and debugging of OSEDA is not guaranteed. Typically, a group of core developers makes public a first version of the tool and stays active for some time processing demands for fixing bugs in reasonable time. However, core developers may at some point withdraw, retire, loose interest, etc., thus the maintenance and debugging risk to be slowed down or totally discontinued. Users then may loose interest in the tool if bugs cannot be fixed or new features cannot be added, and the tool may eventually become obsolete.

OSHW and OSEDA must be extensively validated and verified before usage. The presence of errors and bugs may result in erroneous, lower-performance, and non-manufacturable designs. Ideally, many potential users should play the role of testers to validate and verify the beta versions. However, this is not guaranteed, thus reducing the confidence of the end users and affecting the spreading and popularity of OSHW and OSEDA.

It is unclear if foundries will accept to openly share their PDKs in the context of OSEDA. This is especially true for advanced technology nodes where confidentiality rises. Thus, OSHW and OSEDA in the end may be only linked to old and obsolete technology nodes without offering the possibility of performing state-of-the-art designs.

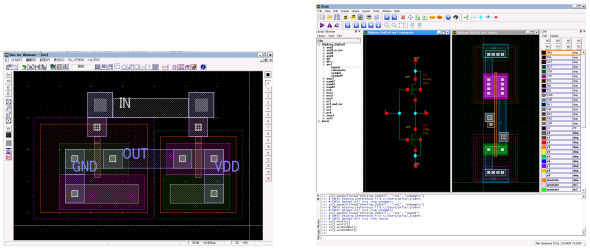
Academia is typically behind the development OSHW and OSEDA, but securing sufficient funding to develop OSHW and OSEDA is not straightforward. It is unclear which bodies (i.e. universities, governments, donors, etc.) will accept to provide generous funding to boost the development of OSHW and OSEDA and whether this funding will be uninterrupted.

Many developers despite being in favor of OSEDA and actually having this goal at the initial stages of the development, in the end they choose rather to pursue a technology transfer or the creation of a start-up since the economic incentive becomes too high. In general, the success of OSHW and OSEDA will largely depend on devoted and knowledgeable volunteers and passionates and on the rise of a spirit of open source consciousness in the design and EDA communities.

IV. Examples of OSEDA and OSHW for AMS Circuit Design and Prototyping

A. MakeLSI: Project

MakeLSI: Project is a project aiming at realizing an open source Large Scale Integration (LSI) design and fabrication community [17]. The project started using the FAIS Semiconductor Center [18], which is a commonly operated LSI fabrication facility in Kitakyushu, Japan. FAIS offers a 2μm, two-metal layer CMOS technology, with a simple and clear lambda-based design rule. Using the PDK does not require signing a NDA and, in addition, the users are free to share and distribute their circuit designs. Finally, the cost to fabricate a wafer is affordable and suitable for training and educational purposes and even for hobbyists.



(a) Wgex (b) Glade

Fig. 1. OSEDA tools used in "MakeLSI: Project".

The project employs two OSEDA tools for physical design, which are accompanied with tutorials so as to guide the user in the first steps of the design. The first OSEDA tool is *Wgex* and is used for layout design with combined circuit extraction and Design Rule Checking (DRC) [19]. The second OSEDA tool is *Glade* and is used for generating and verifying schematics and layout with built-in DRC and Layout Versus Schematic (LVS) [20]. Figs. 1a and 1b show screenshots from these two tools.

The project is running for four years now and in total four fabrication runs have been performed using the FAIS technology. In each fabrication run, several circuits were designed by the members of the project, including analog, radio frequency (RF), and digital circuits, as well as sensors. Fig. 2 shows the microphotographs of two example circuits.

The project now also targets using the 0.6μm technology provided by Phenitec Semiconductor Corp., Japan. Although

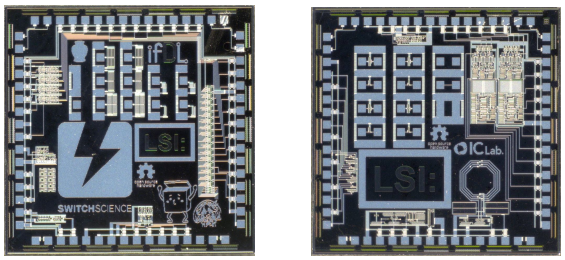
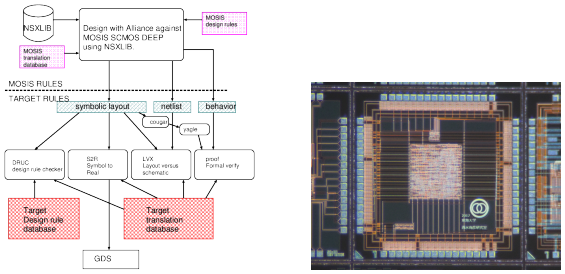


Fig. 2. Microphotograph of chips fabricated in the framework of the "MakeLSI: Project".

using this process requires a strict NDA for design rule disclosure, the project tried to avoid this by using directly the design rules of the FAIS 2μm technology with a shrinking factor of $\times$0.3. Some information has still to be provided by Phenitec Semiconductor Corp., such as contact and via size. MOSFET spice parameters were also fitted from measured fabricated devices, in order to generate the MOSFET simulation model and circumvent relying on the model included in the actual PDK. The MOSFET parameter extraction is performed by the OSEDA tool *PyEDA* [21].

In order to design the digital part of mixed-signal circuits, the project selected the *Alliance* OSEDA tool chain [10] and its included standard cell library. *Alliance* is a complete set of OSEDA tools based on symbolic unit λ, starting at RTL level and going all the way down to layout and GDSII. *Alliance* has a special layout tuning mechanism to migrate a symbolic layout into a real one. Therefore, the layout component dimensions generated with *Alliance* are not constrained to be multiple of λ, unlike other λ-based rule existing tools. This feature makes *Alliance* to be compatible with a wide range of technologies. The project has successfully fabricated LSI chips with *Alliance* using the 180nm ROHM technology [22] and the 0.6μm Phenitec Semiconductor Corp. technology. Fig. 3 shows the design flow and a microphotograph of a fabricated chip [23], [24].



(a) Design flow (b) Phenitec chip

Fig. 3. NDA free design method and the generated chip layout

B. Electrical simulators

Ngspice [25] is one of the most popular mixed-signal circuit simulation tools. Its code is based on three open source software packages, namely *Spice3f5* [26], *Cider1b1* [27], and *Xspice*. It is an ongoing project that stared 15 years go, growing continuously with the help of new contributions suggestions, and reports from users.

C. Analog circuit sizing

Oceane [28] is an OSEDA tool dedicated to the electrical sizing of analog circuits. *Oceane* provides a library of parametrized topologies of several analog functions, i.e. Operational Transconductance Amplifier (OTA), operational amplifier, comparator, voltage regulator, filters, switch, etc. The user has to select a technology, a topology, and set the values of the target performances. *Oceane* provides the sized topology in the form of a *spice* netlist [25], [26] and estimates of the performances, together with a set of benchmarks compliant with *spice* simulation so as to validate the estimated performances. The user can also perform statistical analysis to reach a centered design that will have a high fabrication yield.

D. Field-programmable analog array (FPAA)

FPAA is the analog equivalent of the field-programmable digital array (FPGA) and is perhaps the most popular OSHW platform for rapid and flexible AMS circuit design and prototyping [29], [30]. FPAA can enable configurable and programmable analog and digital computation and interfacing.

E. Benchmarks for analog test

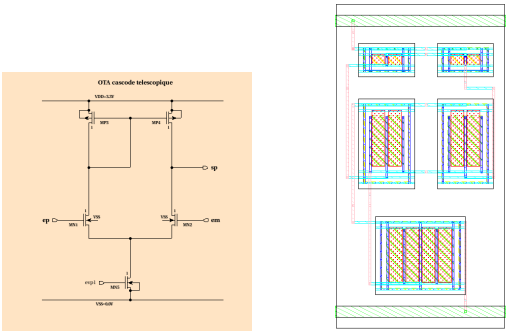
Mentor Graphics and ams AG recently made available a set of benchmark AMS circuits with the aim to facilitate the development of fault models, design-for-test techniques, and test generation techniques, as well as their comparison based on fault coverage metrics and fault simulation times [31], [32]. The list of benchmark circuits includes an operational amplifier, a high-speed comparator, a power-on reset circuit, a charge-pump phase locked loop (PLL), and a 8-bit digital-to-analog converter (DAC). It is hoped that this set of benchmarks will boost the development of alternative, low-cost test techniques for AMS circuits, similarly to what happened for digital circuits following the publishing of digital benchmark circuits [33], [34].

F. SystemC AMS extensions

Virtual Prototyping (VP) is used for the design space exploration and verification of complex and heterogeneous embedded systems [35]. *SystemC* is a hardware description language for rapid VP of digital systems. In the framework of the European Project Catrene/BREAMS [36], the AMS extensions of *SystemC* [37] have been standardized by the Accellera consortium [38] under the OSCI [39] licence. In 2016, a new version of the Language Reference Manual [40] has been standardized by Accellera Systems Initiative [41] under the Apache licence [42], as well as by the IEEE consortium [43]. Version 2.1 of the simulator proof of concept has been recently released by COSEDA [44] compliant with the IEEE standard 1666.1 under the Apache 2.0 licence. *SystemC AMS* adds the Timed Data Flow (TDF) model of computation to SystemC, that handles analog signals sampled in time. The TDF model of computation is inspired by the Synchronous Data Flow model [45]. TDF models can interact with *SystemC* models thanks to converter ports. The *SystemC AMS* TDF model of computation is fully compliant with the discrete event simulator of *SystemC* [46], therefore mixed-signal system VP can be performed within the same simulation environment [47], [48].

G. Place & Route

Coriolis [49] is perhaps the only Place & Route EDA tool to be released as Free Open Source Software (FOSS) under the GPL licence [50]. The ongoing work of the *Coriolis* team is to extend its features to analog and mixed-signal circuits and systems [51]. It is now possible to take a netlist sized with *Oceane* and design the layout with *Coriolis*. Fig 4 shows the netlist of a simple OTA sized with *Oceane* and the corresponding layout designed with *Coriolis*.



(a) *Oceane* Netlist (b) *Coriolis* Layout

Fig. 4. OTA sized with *Oceane* and its layout with *Coriolis*.

H. Layout viewer and editor

KLayout is a GDS and OASIS file viewer and editor [52]. It comes with a comprehensive documentation. It allows the drawing of any shape required by a technology process.

I. OSHW in health applications

echOpen [53] is an open and collaborative project and community, led by a multidisciplinary core of experts and senior professionals with the aim of designing a functional low-cost and open source echo-stethoscope (ultrasound probe) connected to a smartphone, allowing the radical transformation of diagnostic orientation in hospitals, general medicine and medically underserved areas.

V. Conclusion

We argued about the several benefits that OSEDA and OSHW can offer and pointed to the several difficulties that need to be overcome towards this goal. We also shed light on today's status of OSEDA and OSHW specifically for AMS circuit and system design and prototyping. While several OSEDA and OSHW exist and can be used to perform a low-cost design, it will require a larger collective effort to make OSEDA and OSHW trustful and useful in the context of practical and robust designs.

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