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Negative static charge and induced internal electric field have often been observed in the interfaces between silicon and high-κ dielectrics, for example Al_2O_3 and HfO_2. The electric field provides either beneficial (e.g., field-effect passivation) or harmful (e.g., voltage instability) effect depending on the application. Different intrinsic and extrinsic defects in the dielectric film and interface have been suggested to cause the static charge but this issue is still unresolved. Here spectroscopic evidence is presented for a structural change in the interfaces where static charge is present. The observed correlation between the Si core-level shift and static negative charge reveals the role of Si bonding environment modification in the SiO_2 phase. The result is in good agreement with recent theoretical models, which relate the static charge formation to interfacial atomic transformations together with the resulting acceptor doping of SiO_2.

1. Introduction

High-κ dielectric materials, for example, Al_2O_3 and HfO_2, are widely used in silicon-based electronic components where they have replaced traditional silicon oxide SiO_2 in many applications. Si/HfO_2 interface is not only exploited in complementary metal oxide semiconductor (CMOS) transistor manufacturing, but it is also becoming increasingly an important structure for example in ferroelectric nonvolatile memory (FeRAM) applications.[1,2] On the other hand, Al_2O_3 deposition has been recently developed to further improve Si surface passivation in photovoltaic devices.[3] Typically, the interface between Si and high-κ material contains a thin layer of SiO_2 due to energetically favored Si oxidation. Previously it has been found that the post-annealing of Si/high-κ interface can induce a static charge in the material.[4–8] In many applications, the interface charge is considered harmful. However, it is also utilized and developed to passivate silicon solar cells and other state-of-the-art photonic devices in which the internal electric field is used to repel charge carriers deeper into Si bulk away from surface defects.[9–11] Several explanations, for example, crystal defects, broken bonds, and local charge distributions, have been presented to explain the static charge formation and field-effect passivation. The origin of the charge has been related to the Si/dielectric interface rather than the top oxide-gate metal interface.[6,12–16] The formation of the static charge is still an open issue, which has also hindered the controlled use of the phenomenon in technology. The static charge belongs to an interesting area of charge transfer phenomena in which charges are exchanged by two different materials at a junction.[17,18] In this work, we demonstrate the one-to-one correspondence between the static charge formation and the modification of the interfacial SiO_2 bonding structure. We have investigated the Si/high-κ dielectric interfaces after post-annealing in different temperatures under ultra-high vacuum (UHV) or N_2 gas. The static charge was observed by capacitance-voltage (CV) measurements of metal-oxide-semiconductor (MOS) capacitors and corona oxide characterization of semiconductor (COCOS) method.[19] The changes in the SiO_2 bonding structure at the interface were studied by depth profiling with hard x-ray photoelectron spectroscopy (HAXPES) and by ab initio calculations.

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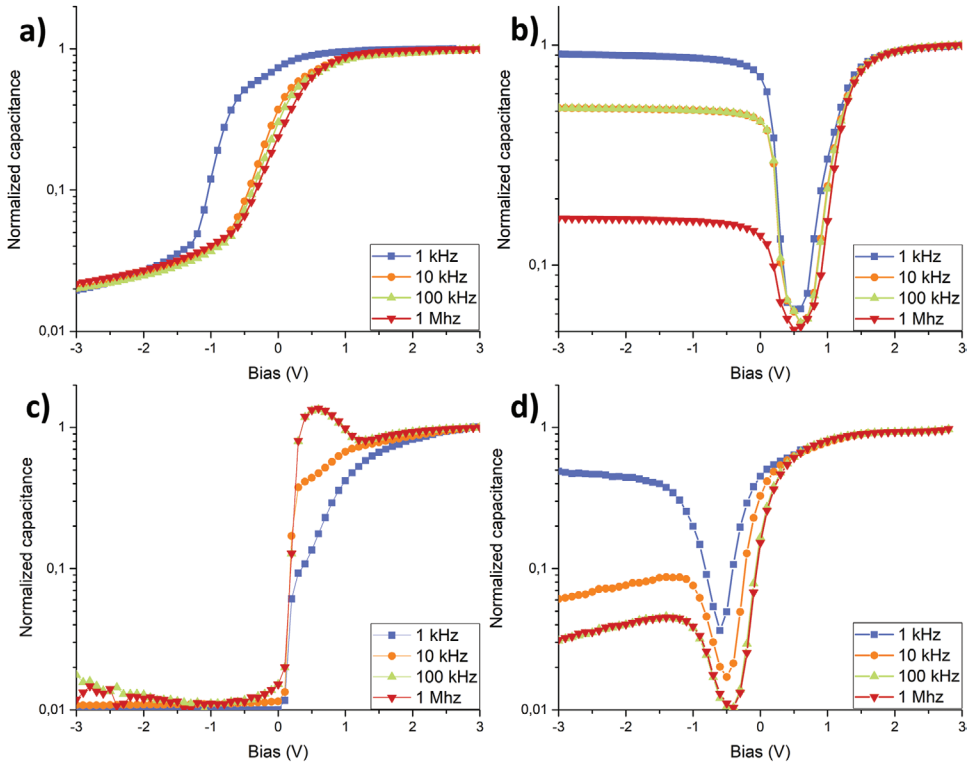

Figure 1. MOS capacitor CV measurements reveal high frequency inversion capacitance after post-annealing. Graphs a, b) are of Al_2O_3 and c, d) of HfO_2 after 300 and 500 °C post-annealing respectively. Substrate material is n-type, that is, inversion occurs with negative bias voltage.

2. Results and Discussion

2.1. Observation of the Negative Static Charge

Static negative charge was observed on the samples by CV measurements after post-annealing. **Figure 1** shows the CV curves of the sample before and after post-annealing. Most importantly, a significant capacitance increase was observed in inversion with high frequencies after the 500 °C post-annealing. Typically, the capacitance increase in inversion is observed only in low frequencies as the minority carriers in the depletion region are able to respond to the measurement signal. An increase in the high-frequency inversion capacitance in Si/high-κ interfaces has been previously reported and explained by static charge at the interface.[4,5,20] It has been also shown that post-annealing causes charge formation.[7] The increased high-frequency inversion capacitance is clear evidence of the static charge in the interface. **Figure 2** illustrates how the high-frequency inversion capacitance is induced by the static negative charge in the interface. The high-frequency inversion capacitance increase at high frequencies (>1 kHz) occurs because the negative charge pulls the minority carriers toward the Si/high-κ interface creating a hole reservoir near the interface, that is, creating a short static depletion region below the interface by pushing majority carriers deeper to the bulk Si. In inversion the layer of minority carriers around the capacitor pad can move between the reservoir and the capacitor depletion region causing the inversion capacitance to increase in high frequencies. The minority carrier layer has earlier been described as "peripheral inversion" and observation of similar hole gas has also been reported earlier.[4,18] Here, the high-frequency inversion capacitance increase is observed only in samples annealed at 500 °C, shown in Figure 1 as an increased capacitance with negative bias voltages. We observed that 500 °C temperature for 600 s is required for the high-frequency inversion capacitance to appear, which is in agreement with the literature.[7] The maximum absolute capacitance of our devices reduces approximately 20% during the 500 °C annealing. The reduction is most likely caused by a small change on the thickness of the stack which is discussed in more detail later. This indicates that the dielectric constant of HfO_2 or Al_2O_3 do not change significantly during the 500 °C annealing. We also confirmed the charge formation with the COCOS method, by which we observed the total charge doubling from $Q_{tot} = -3 \times 10^{11}$ cm^{-2} to $Q_{tot} = -6 \times 10^{11}$ cm^{-2} due

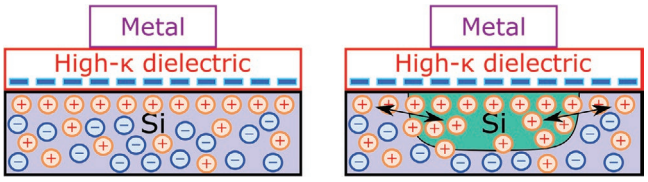

Figure 2. Static charge induced high frequency inversion capacitance formation in the interface. The negative charge in the interface pulls a reservoir of holes in n-type Si close to the interface. In flat band situation (left) the charge induces a small static depletion region in the interface. In inversion (right), the holes in the reservoir are close enough to the surface to contribute to the capacitance in high frequencies, presented with arrows.

to the annealing. Importantly, the COCOS result rules out any additional effects from metal contact, because the sample contains only the Si/high-κ stack. The high-frequency inversion capacitance mechanism is discussed further in the Supporting Information. COCOS method was also utilized to determine the mid-gap state density to be 4×10^{11} cm^{-2} eV^{-1} before and after the annealing. Typically the mid-gap state density reduces during annealing in Si/high-κ materials, but it can also increase in some situations.[7,21] However, the result indicates that interface defects are not related to the negative static charge formation which is also presented earlier.[21] The frequency dependent dispersion in Figure 1 and the rising feature in Figure 1c are most probably effects of the interface defects.[4] The differences between the samples are observed because the defect level distribution around the energy gap is different for Al_2O_3 and HfO_2 and it can change during annealing. Detailed analysis of the defect induced CV characteristics is outside of the scope of this study.

2.2. Investigation of the Interface Electronic Structure

The electronic structures of the interfaces were studied with HAXPES measurement to understand the origin of the static negative charge. **Figure 3** shows a comparison of Si 2p spectra of the samples with static charge annealed to 500 °C and reference samples annealed to 300 °C measured at different depths of the stack. In the reference sample, the silicon oxide peak corresponds well to the +3- and +4-oxidation state components at +2.62 and +3.67 eV respectively, which arises from the native SiO_2.[22] Native SiO_2 forms on the interface during the initial stages of ALD when the Si surface reacts with the oxidizer precursor and during the post-annealing when the interfacial Si reacts with the high-κ material or with interstitial oxygen inside the insulator. In contrast, the samples with static charge have a separate higher binding energy component at +4.30 eV in addition to the other oxidation state components. The higher binding energy component can be distinguished from both Si 2p and Si 1s spectra. The higher BE component is unique to the samples with static charge; thus, it originates from the 500 °C post-annealing.

Further analysis of Al 2p, Hf 4f, and O 1s spectra in **Figure 4** shows only small differences, however, HfO_2 samples have a clear increase in O 1s tail in high binding energy after high-temperature annealing. The high binding energy tail originates from the oxygen in SiO_2. The tail can be observed only in HfO_2 samples because the binding energy for O 1s is higher for oxygen in Al_2O_3 compared to HfO_2.[23,24] The tail overlaps with the main peak in Al_2O_3 samples hiding it. Additionally, Al 1s and Hf 3d spectra were analyzed, but no significant differences related to annealing were observed. Notably, the samples with static charge contain more SiO_2 in the interface, which contributes to the stack thickness causing the absolute capacitance of the stack to decrease. This can be a result of silicon reacting with the oxygen in the alumina or hafnia. In these reactions, silicon may react with oxygen from the oxide, or the high-κ films may contain additional interstitial oxygen, which reacts with Si in the interface. The oxygen could also diffuse through the film during the post-annealing, although it is unlikely.[25] However, this effect is ruled out by the UHV annealing in which oxygen diffusion from outside is not possible. Moreover, the increased SiO_2 layer in the interface is not thick enough to explain the charge formation alone.[26] In summary, the observed changes in the electronic structure suggest that structural modification happens in the interface during annealing. The structural modification occurs most likely because of reaction between the Si, the SiO_2 and the high-κ material in the interface. This structural modification

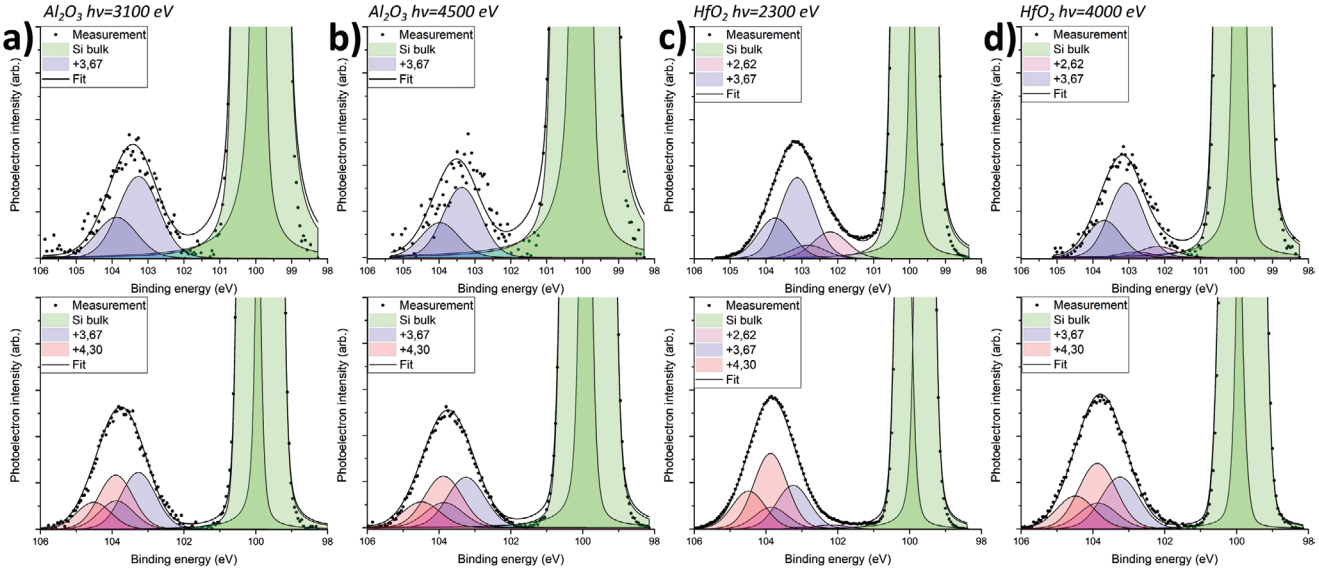

Figure 3. Si 2p photoelectron spectra. Reference samples (top row, 300 °C post-annealing) contain mostly +4 oxidation state seen as +3.67 eV component. Samples with static charge (bottom row, 500 °C post-annealing) contain also a unique component at +4.30 eV, which is related to the static charge formation. The selected photon energies probe the stack at the vicinity of the interface. IMFPs are a) 4.9 nm for 3100 eV, b) 6.6 nm for 4500 eV, c) 3.9 nm for 2300 eV, and d) 6.0 nm for 4000 eV.

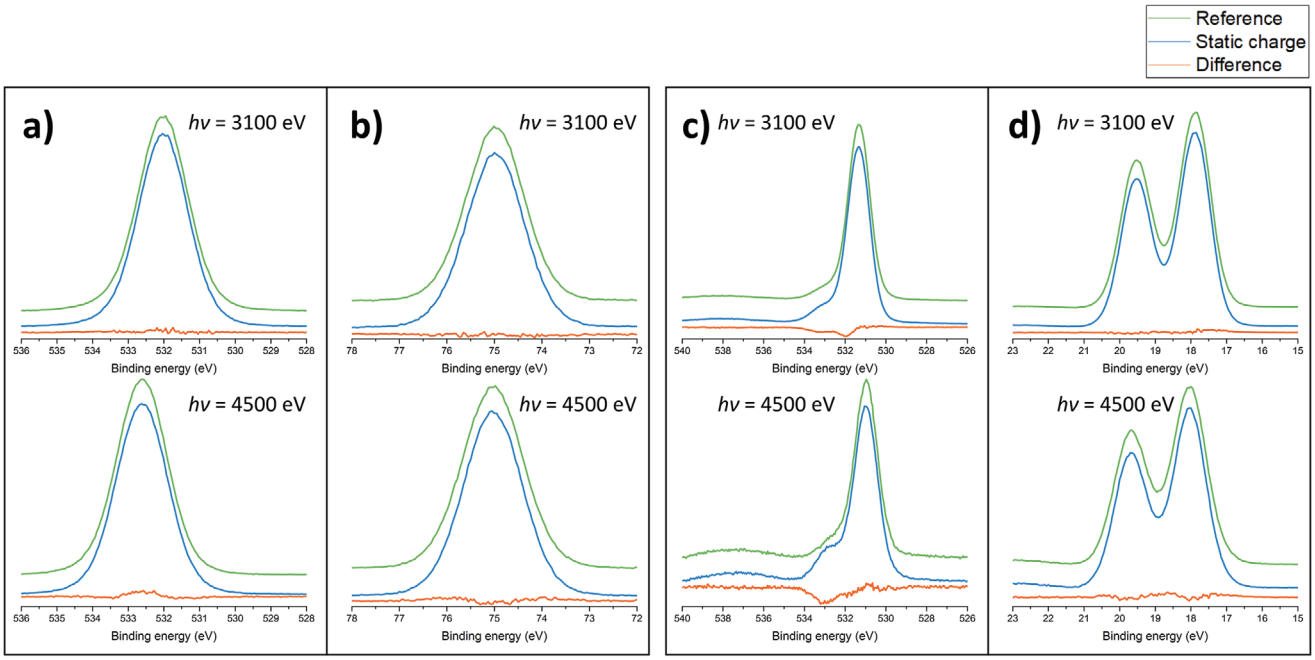

Figure 4. Comparison of Al 2p (b), Hf 4f (d), and O 1s (a and c respectively for Al_2O_3 and HfO_2) spectra: reference sample spectra (top, green) are subtracted from the static charge sample spectra (middle, blue). The difference is shown at the bottom (orange). Higher binding energy tail in O 1s spectra is observed in HfO_2 samples while this feature is hidden in Al_2O_3 samples due to overlapping of peak components. Al 2p and Hf 4f spectra have no significant difference between static charge and reference.

relates to the static charge formation as it is observed systematically in those samples.

2.3. Computational Modeling of the Interface

To understand the HAXPES result and the structural modification, we studied the interface mixing in high-κ/SiO_2 structures by ab initio calculations. Previously has been shown that the interface is relatively stable during annealing, but reactions between SiO_2 and high-κ material can occur.[27,28] It has been also shown that bonds between Si and metal atoms in the interface can be energetically favorable.[29,30] We studied several intermixed structures with DFT calculations to understand and confirm the role of intermixing in the binding energy shift. The study was limited to the HfO_2/SiO_2 system because it allowed us to build the structure models using a well-known method and to avoid uncertainty presented by the amorphous nature of Al_2O_3.[31] In our experiments, we expect that both Al_2O_3 and HfO_2 dielectrics are amorphous even after the 500 °C annealing as the oxide is not thick enough to allow crystallization.[32] However, the use of the ordered structure to model this type of interfaces has been previously justified even if the interfaces are non-abrupt or contain sub stoichiometric oxides.[16]

Electrostatic potential was calculated from the relaxed structures and it was used to estimate the binding energy shifts in the photoemission spectra. The electrostatic potential was corrected with the Fermi energy from each calculation to allow direct comparison. The calculated electrostatic potentials are presented in **Figure 5**. Average electrostatic potential was used

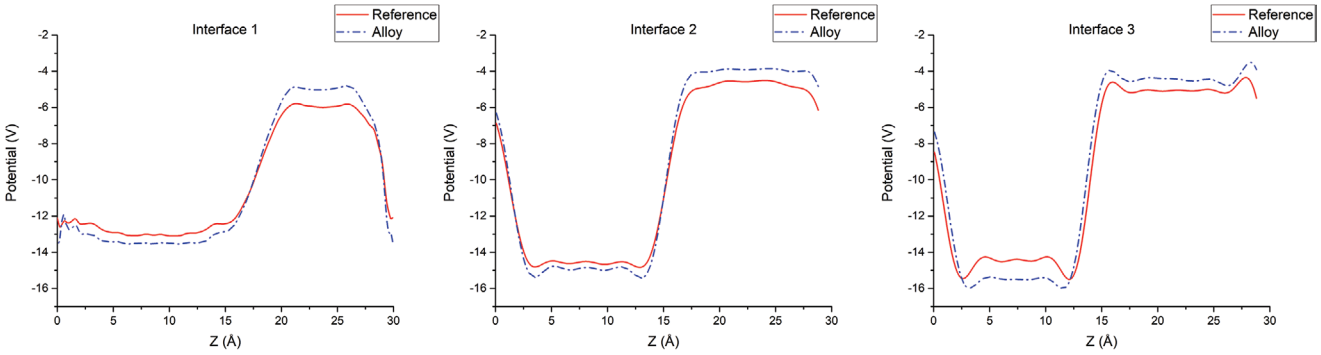

Figure 5. Electrostatic potentials of the relaxed interface structures. The potential is an average calculated from the middle of the unit cell in a direction perpendicular to the interface. The binding energy shift is seen as a higher potential step along with the interface in the models with alloyed structure

to estimate the binding energy shift in the SiO_2 layer. The average electrostatic potential was on average 1 eV higher along the SiO_2 layer in the intermixed interface compared to the non-mixed interface. Thus, we observe the electrostatic potential difference, that is, binding energy shift, throughout the SiO_2 layer. However, this is not the case in the experimental samples, where the bonding structure is not uniform throughout the surface and the SiO_2 layer is thicker compared to the computational case with periodic boundary conditions. Thus, we observe all +2.62, +3.67, and +4.30 eV components in the experiments. Furthermore, analysis of the electrostatic potential in atom positions was used to rule out effects such as natural dipole of the material interface. Potentials from atoms in different positions of the cell were compared to rule out any local effects. Differences in local potentials were only 0.1 eV, which is much smaller than the observed core-level shift. Thus, we conclude that the alloying and short-range bonding changes cause the observed binding energy shift, and simultaneously we can rule out the interface effect. Determining the exact interface structure of the experimental samples is difficult, and most likely it is not well defined. However, studying different interfaces provides an instructive insight into the interface.

The formation of the long-range internal electric field extending from the Si/high-κ interface to deep into the Si crystal is explained by a recent model which is in agreement with our results.[33] Alloying or doping of SiO_2 by Al or Hf atoms in annealing-induced intermixing causes the acceptor type electron levels in the large 9 eV bandgap of SiO_2. Electron transfer from silicon to the acceptor levels causes the static negatively charged levels that induce the internal electric field.[33] Moreover, our experimental results are not consistent with the models where the contamination or the intrinsic defects are suggested to be the origin of the negative charge. No significant carbon or nitrogen contamination was observed in HAXPES measurement after 500 °C post-annealing. Additionally, oxygen/aluminum and oxygen/hafnium intensity ratios do not change after 500 °C post-annealing, which supports that the intrinsic defects, that is, interstitials or vacancies hardly have a role in the charge formation. To conclude, no other one-to-one correspondence, in addition to the Si core level shift, was observed in HAXPES measurement.

3. Conclusions

To summarize, we have investigated the static charge formation in the Si/high-κ interface. The charge forms during the 500 °C high-temperature post-annealing in N_2 background or in UHV, consistent with many previous results.[4–7] High-resolution HAXPES measurement reveals a separate Si oxide component, which correlates with the formation of the negative static charge. This component appears at +4.30 eV after the 500 °C annealing as more silicon oxide forms at the interface because of reaction between Si and the high-κ material and the silicon oxide alloys with the high-κ material. The component is unique to the samples with the static charge. Our DFT calculations of different possible interface structures show that the +4.30 eV arises from alloying of the high-κ and SiO_2 materials at the interface. Our results are well consistent with the recent model demonstrating electron transfer from Si to the Al-doping induced acceptor levels in the interfacial SiO_2.

4. Experimental Section

Samples (6 × 12 mm) were cut from n-type Si(100) wafer (phosphorus-doped, 3–9 Ω cm). Samples were prepared with RCA clean and dip to 5% HF solution to remove contaminants and Si oxides and to H-passivate the surface prior to loading into atomic layer deposition (ALD) equipment. High-κ dielectrics, Al_2O_3 and HfO_2, were grown to the sample with ALD. The ALD precursors were trimethylaluminum and H_2O for Al_2O_3 and tetrakis(dimethylamido)hafnium and H_2O for HfO_2. Sample temperatures during growth were 180 and 130 °C for Al_2O_3 and HfO_2 respectively and pulse time of 1 s was used for all ALD growths. A film thickness of 5 nm was used which was confirmed from all samples with an ellipsometer. The samples were post-annealed at 500 °C for 10 min after ALD to generate the static charge. Reference samples were post-annealed at 300 °C to improve the Si/high-κ interface. Post-annealing was done in a wafer oven under N_2 flow or in a UHV system at 10^{-9} mbar pressure, which both produced similar results. Selected samples were measured with XPS after ALD process and annealing to rule out the possibility of contamination during annealing. Samples for HAXPES and COCOS measurements were prepared without metal contacts to avoid any interference with the measurement. Special care was taken to avoid contamination and its effect on the results as is described in the Supporting Information.

For CV measurements, MOS-capacitors were fabricated from the Al_2O_3 and HfO_2 coated samples by sputter-coating 200 µm circular Cr/Au pads with a shadow mask on top of the insulator material. Samples were characterized by CV measurement with HP4284A LCR meter. In CV-measurements, a frequency range of 1 kHz–1 MHz was used with a 20 mV AC signal to observe the capacitance dependence on frequency.

In order to study the charge formation further, the materials were measured with HAXPES at the GALAXIES beamline in SOLEIL, Paris, France.[34] Measurement was a non-destructive depth profile of the stack, in which the target was to study changes in oxidation states of Si and high-κ material through the stack. Photon energies in the range of 2.3–6.9 keV were used to reach inelastic mean free paths (IMFP) of 3.9–9.3 nm in the stack.[35] The estimated energy resolution was 300 meV at 2.3 keV beam energy with Si(111) monochromator and 200 meV at 6.9 keV with Si(333) monochromator. Maximum photon flux to the sample during the measurement was 10^{12}–0^{13} photons/s. Samples were measured with a grazing incidence beam of 1° and 10° to improve photoelectron intensity. Fitting of the spectra was done with the Origin 2016 program using Shirley background shape to remove the inelastic background and Voigt line shape to fit the spectra. Binding energy shifts for silicon oxide which were used in fitting are listed in the literature.[22,36] Au 4f spectra were measured with each beam energy for binding energy calibration. Although the Au 4f spectra allowed to determine the exact beam energy, additional calibration was needed for each sample to take thin film charging effects into account. The Si 2p bulk peak was observed within a width of 0.03 eV for all the samples measured at each photon energy, which excludes any possible broadening or shifting effects caused by the sample charging during the measurement.

DFT calculations were performed with the VASP program using the projector augmented plane wave method (PAW) with PBE potentials. The structure models were constructed by rotating cubic HfO_2 cell 45 degrees to match the lattice constant of cubic β-cristobalite SiO_2 cell.[31] The method provides an easy way to build interfaces that comply with electron counting rules and provides very little initial strain in the interface. In the models, the SiO_2 was expanded to fit the cubic HfO_2 cell a = 7.30 Å. The interface mixing was introduced by symmetrical substitutions in the interfaces. Three different models were constructed which are presented in the Supporting Information. The models were relaxed in the calculation to 0.05 eV $Å^{-1}$ cutoff. Plane wave cutoff was set to 500 eV to avoid the Pulay stress effect in the bulk calculation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

high-κ dielectrics, interface static charge, interfaces, semiconductors

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