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Khalil Chennit, Najmeh Delavari, Samia Mekhmoukhen, Rassen Boukraa, Laure Fillaud, et al.. Inkjet-Printed, Coplanar Electrolyte-Gated Organic Field-Effect Transistors on Flexible Substrates: Fabrication, Modeling, and Applications in Biodetection. *Advanced Materials Technologies*, 2023, 8 (2), pp.2200300. 10.1002/admt.202200300 . hal-03820671

HAL Id: hal-03820671

<https://hal.sorbonne-universite.fr/hal-03820671>

Submitted on 24 Nov 2022

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Inkjet-Printed, Coplanar Electrolyte-Gated Organic Field-Effect Transistors on Flexible Substrates: Fabrication, Modeling, and Applications in Biodetection

Khalil Chennit, Najmeh Delavari, Samia Mekhmoukhen, Rassen Boukraa, Laure Fillaud, Samia Zrig, Nicolas Battaglini, Benoît Piro, Vincent Noël, Igor Zozoulenko,* and Giorgio Mattana*

The first example of inkjet-printed, electrolyte-gated organic field-effect transistors, fabricated on flexible polyimide substrates is presented. The interdigitated source and drain electrodes, and the coplanar gate electrodes, are inkjet-printed using a homemade gold nanoparticle ink. A semiconducting ink based on the p-type, organic semiconductor poly[2,5-(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno [3,2-b] thiophene)] (DPP-DTT) is formulated and inkjet-printed onto the channel. The performances of inkjet-printed, coplanar devices are compared to those of transistors whose gate electrode consists in a metallic wire inserted in the electrolyte. Printed transistors show excellent electrical properties with field-effect mobility as high as $0.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The electrical behavior of inkjet-printed, coplanar devices is also modeled using the Nernst–Planck–Poisson (NPP) equations, where the output and transfer curves are calculated based on the charge and potential distribution inside the device. Good quantitative agreement between the simulation and experiments is achieved, outlining the attainable use of NPP simulations as predictive tools for device design and optimization. To demonstrate an example of application, printed transistors are functionalized for the detection of complementary DNA strands. This study opens an avenue for the next generation of low-cost, flexible sensors and circuits, both through experimental studies and device modeling.

1. Introduction

Organic bioelectronics is a new, interdisciplinary, emerging branch within the field of organic electronics. In a very broad sense, it may be defined as the use of organic electronic devices in biological systems^[1] to monitor or even stimulate the activity of living organisms.^[2] Organic materials seem particularly suitable for the development of interfaces between electronics and biology because of their unique mechanical properties as well as their ability to conduct ions, in addition to electrons and holes.^[2,3] Besides other optimal characteristics in terms of cost and performances, ideal devices for organic bioelectronics should satisfy further requirements, for instance in terms of flexibility/conformability and the possibility to work in liquid environments.^[2,4] These requirements are particularly important for those applications necessitating the operation of organic devices on moist, highly non-planar surfaces such as, for instance, in the field of wearable skin chemical sensors^[5] or implantable bioelectronics.^[6]

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The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/admt.202200300>.

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DOI: 10.1002/admt.202200300

Among the different types of organic electronic devices currently employed in the field of organic bioelectronics, an important role is played by the electrolyte-gated organic field-effect transistors (EGOFETs). EGOFETs have emerged as a new subset of organic field-effect transistors (OFETs) in the last fifteen years.^[7] Contrary to “traditional” OFETs, where the organic semiconductor (OSC) and gate electrode are separated by a thin layer of a solid-state dielectric, in EGOFETs the capacitive coupling between the gate and OSC is achieved thanks to an electrolyte, in liquid or in gel phase^[8,9] or even pure water.^[10] The intrinsic presence of a small volume of electrolyte (typically a few tens of microliters) in the transistor structure, combined with the very small polarization voltages (typically <1 V) necessary to bias this type of transistors, makes EGOFETs ideal candidates for the fabrication of low-power sensors for the detection of molecules in liquid media.^[7] The core of an EGOFET device is represented by two interfaces, the first one located between the gate and the electrolyte, the second one between the electrolyte and the OSC. When one of these two interfaces is properly functionalized by a receptor, the binding of target molecules results in a modification of the corresponding capacitance which, in turn, modifies the gate/OSC total capacitance.^[11–14] Since the current flowing between the source and drain electrodes is a function of this total capacitance, when this capacitance changes, the transistor’s output current changes accordingly, therefore the detection of the target molecules/reaction produces a measurable variation of the transistor’s output current. So far, EGOFETs have been successfully used for the detection of different types of biological analytes in liquid media such as: ions,^[13,15] DNA,^[12,16] streptavidin,^[17,18] organic chiral compounds,^[19] and cytokines^[20] just to mention a few recent examples.

The large majority of EGOFETs and EGOFET-based sensors reported so far in the literature are fabricated on rigid substrates (silicon/SiO₂ wafers, glass, or quartz are typical examples), their electrodes being usually deposited by means of thermal evaporation while spin-coating is often employed for the OSC deposition; as such, they are hardly suitable for bioelectronic applications requiring conformal coating.

Printing deposition techniques, which allow fabrication of devices on lightweight, flexible and/or conformable substrates, represent a potential solution to overcome this issue.

Printing techniques have long been used for the fabrication of organic devices and circuits.^[21] Besides the aforementioned possibility of using flexible substrates, additional advantages connected to printing techniques are the decrease of fabrication costs, a more efficient use of fabrication materials, and the realization of devices on large areas.^[22]

Among the different printing techniques, inkjet-printing has recently attracted considerable attention, especially for the fabrication of organic transistors.^[23] Inkjet-printing is unique in the field of printed electronics as it is an additive, digital, non-contact deposition technique that can be easily adapted to any size of production scale.^[23,24] While examples of all-inkjet-printed OFETs and organic electrochemical transistors (OECTs) are more and more commonly reported in the literature,^[25–29] this is much less the case for EGOFETs. Inkjet-printing has indeed been used in a few fabrication steps, for instance for the deposition of the source and drain electrodes,^[30] the polyelectrolyte^[31] or the OSC.^[32] Wang et al.^[33] described an EGOFET structure fabricated on flexible poly(ethylene terephthalate)

(PET) foils where the electrodes and the semi-conducting layer were all deposited by inkjet-printing; however, the electrical characterization of such devices is not reported in the article and nothing is said about their transistor behavior. It seems therefore, to the best of our knowledge, that an example of functional EGOFETs where both the electrodes and the semiconductor are deposited by inkjet-printing on a flexible substrate has never been presented.

The fabrication of inkjet-printed EGOFETs or EGOFET-based biosensors requires profound modifications of their geometry. EGOFETs are typically realized by fabricating the source and drain electrodes on the same plane and by covering the channel area with a thin film of organic semiconductor. Then, on the top of the OSC, a drop of electrolyte is deposited and the gate electrode (usually in the form of a metallic wire) is dipped inside the electrolyte, along a direction which is perpendicular to the plane containing the source and drain. If one aims at making a device in which all electrodes are inkjet-printed, this approach may not be followed as one would need all the printed layers to lie on (or to be parallel to) the same plane. A possible solution to this problem may be represented by a new design called “coplanar structure” in which the three transistor electrodes are deposited on the same substrate, the gate being a conductive stripe placed next to or surrounding the channel area. This configuration, quite common for organic electrochemical transistors (OECTs), has been very rarely utilized for the fabrication of EGOFETs. It was first proposed by Yaman et al. in 2014^[34] and was employed a few years later by Leonardi et al.;^[35] in both cases, electrode deposition was performed by conventional photolithographic techniques. If one is unable to finely control the OSC deposition over the channel area, the presence of a coplanar gate may increase the complexity and number of steps of the transistors’ fabrication process to avoid direct contact between the gate and the OSC. Thus, one may be obliged to physically scratch the excess of semiconductor accidentally deposited on the gate^[34] or directly protect the gate surface with a sacrificial layer prior to OSC deposition.^[35]

In this paper we describe functional, coplanar EGOFETs fabricated on flexible polyimide foils where all the electrodes and the semiconductor are deposited by exclusive means of inkjet-printing. The source, drain and gate electrodes are fabricated in a coplanar configuration, using a homemade suspension of gold nanoparticles. On the interdigitated source/drain structure, a thin layer of poly[2,5-(2-octyl-dodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno [3,2-b]thiophene)] (DPP-DTT) is also inkjet-printed. It should be noted that inkjet-printing allows a highly controlled deposition of the OSC only on the channel area: no protective sacrificial layers or post-deposition electrode cleaning are needed to avoid undesired semiconductor presence on the gate surface.

To better understand the influence of the OSC deposition technique but also that of the coplanar structure on the overall electrical performances of the devices, four different types of transistors are here presented and characterized:

Type 1 (3D-DC): devices where the OSC is deposited by means of drop casting, the gate electrode is a gold wire dipped into the electrolyte;

Type 2 (3D-IJ): devices where the OSC is deposited by means of inkjet-printing, the gate electrode is a gold wire dipped into the electrolyte;

Type 3 (2D-DC): devices where the OSC is deposited by means of drop casting, the gate electrode is deposited around the channel area by inkjet-printing;

Type 4 (2D-IJ): devices where the OSC is deposited by means of inkjet-printing and the gate electrode is deposited around the channel area by inkjet-printing (inkjet-printed coplanar devices).

All four types of transistors are fully characterized, in terms of output and transfer curves, and the most important electrical parameters (threshold voltage, charge carriers' mobility, I_{ON}/I_{OFF} ratio) are extracted and compared.

Moreover, in order to understand and analyze the performance and operation of coplanar EGOFTs (types 2D-DC and 2D-IJ), we perform device modeling based on the approach utilizing the Nernst–Planck–Poisson (NPP) equations that was developed in our recent paper^[36] and that describes on equal footing both the polymer and the electrolyte regions of the device. The output and transfer curves are calculated and analyzed based on the charge and potential distribution inside the device. Good quantitative agreement between the simulation and the experiment is achieved, which outlines the attainable use of NPP simulations as a predictive tool for the device design and optimization.

Finally, to practically demonstrate an example of application, we functionalize the inkjet-printed gold electrode (2D-IJ) with a thiolated single-stranded DNA (ssDNA) aptamer and demonstrate the capability of the functionalized device to detect complementary DNA sequences in the electrolyte.

Our study may contribute to the development of the next generation of low-cost, low-power consumption and flexible devices and sensors, both through experimental studies and device modeling.

2. Experimental Section

2.1. Materials

Devices were fabricated on polyimide foils (Kapton Type HN, 125 μm , purchased from DuPont). Poly[2,5-(2-octyl-dodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno [3,2-b] thiophene)] (DPP–DTT) was purchased from Ossila Ltd, UK ($M_w = 87$ kDa, PDI = 4.1). PBS (pH = 7.4 at 25 $^\circ\text{C}$) was used as electrolyte. The oligonucleotides (thiolated anti-BPA ssDNA aptamer [sequence: 5' to –3'] and complementary DNA [sequence: 5' to –3']) were purchased from Eurogentec, Belgium. All the reagent-grade solvents were purchased from Sigma-Aldrich and used as received.

2.2. Inks Preparation

The formulation of the Au nanoparticle ink used for the fabrication of the transistors' electrodes had been published.^[37]

The semiconducting ink was prepared by dissolving the DPP–DTT powder in 1,2-dichlorobenzene (5 mg mL⁻¹). The solution was kept at 110 $^\circ\text{C}$ under stirring until complete dissolution of the powder occurred (≈ 20 min). It was then cooled down to room temperature before being directly injected

into the cartridge (no filtration was required) or before drop-casting.

2.3. Substrate Preparation

Kapton sheets were cut into squares (10 cm \times 10 cm), washed with acetone and ethanol followed by deionized water and then dried under argon. Prior to inkjet-printing, substrates were thermally treated at 180 $^\circ\text{C}$ for 1 h in a convection oven, in air, to dehydrate their surface.

2.4. Inkjet-Printing

Printing was performed using a Dimatix Fujifilm DMP-2800 printer with 10 pL drops cartridges.

2.4.1. Au electrodes

Electrodes were printed using a drop spacing of 15 μm , a waveform called Waveform 1 was used (Figure S6 and Table S1, Supporting Information). To improve homogeneity, three gold layers were printed one on the top of the other, with a sintering step (220 $^\circ\text{C}$ for 1 h) after each layer printing.

2.4.2. OSC

Prior to the deposition of DPP–DTT, the substrates containing the electrodes were cleaned for a few minutes by exposure to UV-ozone cleaner. They were then dipped in pure ethanol for 5 min to deoxidize gold.

Inkjet-printing of the OSC was performed using the Waveform 2 (see Figure S7 and Table S2, Supporting Information) and a 30 μm drop spacing was chosen, to improve the film homogeneity. Five layers were printed one on the top of the other (delay time of 60 s) and annealed at the end of the printing process in a convection oven at 120 $^\circ\text{C}$ for 1 h, in air, to speed up solvent evaporation and improve the OSC morphology.

2.5. Drop Casting of the OSC

Prior to the deposition of DPP–DTT, the substrates containing the electrodes were cleaned for a few minutes by exposure to UV-ozone cleaner. They were then dipped in pure ethanol for 5 min to deoxidize gold.

Drop-casting was performed by depositing 50 μL of the OSC solution on the channel area (to cover it completely) and dried at ambient conditions overnight; after drying, an annealing process at 120 $^\circ\text{C}$ for 1 h in a convection oven was performed.

2.6. Morphological Characterization of Printed Layers

The morphology of printed layers was investigated by AFM (model NT-MDT Solver P47) using standard silicon probes

(Nanosensors, model PPP-NCHR). AFM images were obtained in the intermittent contact mode and were analyzed with the free software WSxM.^[38]

2.7. Electrical Characterization of EGOFETs

Electrical characteristics were recorded at room temperature using a Keithley 4200 Semiconductor Characterization System.

Two types of curves were acquired: 1) the output characteristics (or I_D - V_{DS} curves): the drain-source voltage difference V_{DS} was swept between 0 and -0.5 V with steps of $\Delta V_{DS} = -0.01$ V. During the acquisition of each output curve, the gate-source voltage difference V_{GS} was kept constant and then decreased in correspondence with the acquisition of the next curve (gate-source voltage range: 0.0 to -0.7 V, step width $\Delta V_{GS}: -0.1$ V); and 2) the transfer characteristics (or I_D - V_{GS} curves): the drain-source voltage difference V_{DS} was kept at a constant value of -0.5 V while the gate-source voltage difference V_{GS} was swept between 0 and -0.7 V (forward curve, $\Delta V_{GS} = -0.01$ V) and then from -0.7 back to 0 V (backward curve, $\Delta V_{GS} = +0.01$ V). In both cases, the drain current I_D as well as the gate current I_G were recorded.

For 3D-DC and 3D-IJ devices, the V_{GS} voltage was applied between the source and a glass-sealed gold electrode (diameter: 250 μm) directly dipped into the electrolyte well, the printed gate electrode was left floating; for 2D-DC and 2D-IJ devices, the V_{GS} voltage was applied between the source and the printed gate electrode surrounding the channel area.

2.8. Device Modeling

To simulate experimentally fabricated devices the authors used an EGOFET model developed in their previous paper^[36]

utilizing Nernst-Planck-Poisson equations that describes, on equal footing, both the polymer and the electrolyte regions of the device. The experimentally fabricated coplanar EGOFET is modelled within a 2D model geometry as shown in Figure 1a,b.

The model consisted of two main regions, namely the OSC, and the electrolyte on top of it. The source and drain electrodes were placed at the bottom of the OSC region (positioned corresponding to the geometry of the electrodes in the actual device) and the gate electrodes were placed at the boundaries of the electrolyte region (Figure 1c). The dimensions A, B, C, L in Figure 1a,b corresponded to the dimensions of the actual fabricated device. Note that 2D modeling was performed, that is, the device was effectively infinite in the y -direction.

Within the model, the electrolyte was ionically conductive and the organic semiconductor was only electrically conductive, that is, ions do not penetrate the polymer region. This ion transport is described by the Nernst-Planck equations (often also called drift-diffusion equations, Equation (1), coupled with the Poisson equation (Equation (2)):

$$J_{c_{\pm}} = -D_{c_{\pm}}(\nabla c_{\pm} \pm f c_{\pm} \nabla V) \quad (1)$$

$$-\frac{\epsilon \nabla^2 V}{F} = c_+ - c_- \quad (2)$$

where c_{\pm} , $D_{c_{\pm}}$ are the concentrations and the corresponding diffusion coefficients for the cations (+) and anions (-), respectively. $J_{c_{\pm}}$ is the flux of ions and $f = F/RT$ (F the Faraday constant, R the ideal gas constant, T the temperature), and V is the electrostatic potential throughout the whole model. For the organic semiconductor region, the hole transport is similarly described by the Nernst-Planck equations coupled with the Poisson equation:

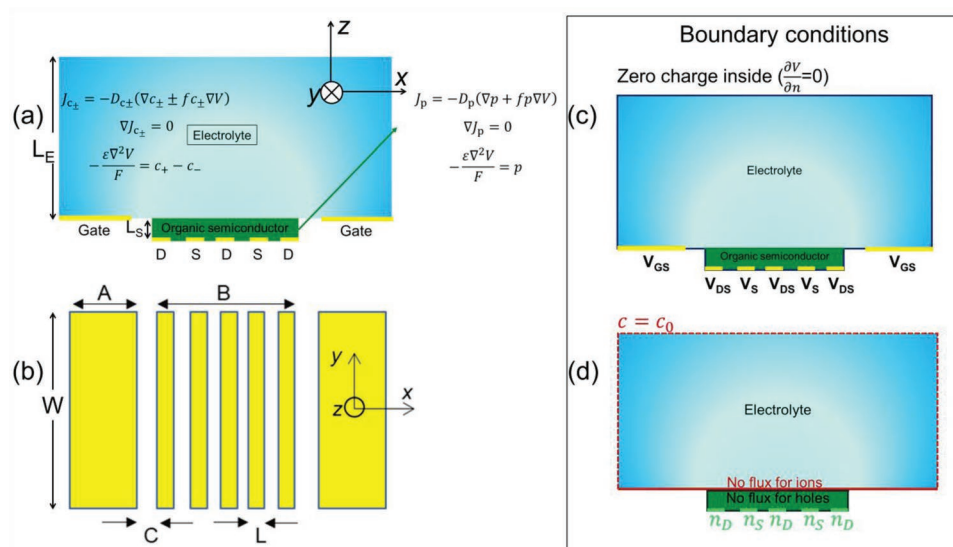


Figure 1. Geometry of the 2D-IJ EGOFET and equations involved in the simulations: a) view from the side, b) view from the above. “S” and “D” denote source and drain electrodes, respectively. Dimensions A, B, C, and L in (b) are the same as indicated in Figure 3a and Section 3.1. All the device dimensions and parameters are specified in Table S3, Supporting Information. c) Boundary conditions for the electric potential V , d) boundary conditions for ions and holes in the electrolyte and in the OSC.

Table 1. Summary of the most important electrical figures of merit of the four types of EGOFETs.

Device code	V_{TH} [V]	μ [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	I_{ON}/I_{OFF} [-]
3D-DC	-0.44 ± 0.01	0.046 ± 0.006	10^3
3D-IJ	-0.43 ± 0.01	0.016 ± 0.001	10^2
2D-DC	-0.42 ± 0.04	0.019 ± 0.001	10^2
2D-IJ	-0.435 ± 0.003	0.017 ± 0.006	10^2

$$J_p = -D_p (\nabla p + fp \nabla V) \quad (3)$$

$$-\frac{\epsilon \nabla^2 V}{F} = p \quad (4)$$

where p and D_p are the concentration and diffusion coefficient for holes, respectively. The mobility (related to the diffusion coefficient as $\mu_p = \frac{D_p}{RT}$) is also dependent on the electric field (based on Poole–Frenkel model, see Equation (5)).^[39]

$$\mu = \mu_p \exp\left(\frac{\gamma \sqrt{E}}{kT}\right) \quad (5)$$

where γ is the Poole–Frenkel constant and E is the electric field.^[40] Note that μ_p is the input parameter of the theory, and in the calculations the authors used experimentally extracted value $\mu_p = 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; see Table 1.

The boundary conditions used in the model are as follows. For the electric potential V in the semiconductor region, the source was grounded ($V_S = 0 \text{ V}$), and the drain potential V_{DS} was applied to the drain electrodes (see Figure 1c). The gate voltage V_{GS} was applied to the gate electrodes placed in the electrolyte region. The boundary condition for all other outer boundaries was set to $\frac{\partial V}{\partial n} = 0$ corresponding to a zero charge inside the device region.

The boundary conditions for hole density in the organic semiconductor region was set at source and drain electrodes to $n_s = n_D = 10^{-7} \text{ mol m}^{-3}$. It is noteworthy that n_s was the only phenomenological parameter used in the present calculations. Its value was chosen to achieve the best agreement between the calculated and measured currents. Therefore, it could also be considered as the outcome of the present modeling, providing the hole density in the semiconductor region by fitting the experimental results. All other boundaries of the organic semiconductor region (including the boundary with the electrolyte) were set to “no flux” boundary condition forbidding a penetration of holes into the electrolyte.

The boundary condition for ions in the electrolyte is defined as a fixed ionic concentration $c_0 = 138 \text{ mol m}^{-3}$ corresponding to the experimental concentration of the electrolyte (dashed red line in Figure 1d). At the lower electrolyte boundary, “no flux” boundary condition blocking ion penetration into the electrolyte region condition was used (solid red line in Figure 1d). It should be noted that utilization of the boundary conditions for ions in the electrolyte as a fixed ionic concentration c_0 could lead to artifacts for certain device geometries (e.g., for the case of small gates) resulting in the violation of the overall charge

neutrality.^[37] In this case, time-dependent calculations with “no-flux” boundary conditions should be used. For the present device geometry, the authors verified that the charge neutrality was satisfied, and the stationary calculations based on Equations (1) to (4) with the fixed ionic concentration boundary conditions lead to the results, identical to those based on the time-dependent calculations.

The current passing through the drain contact (drain current I_D) is calculated by the integration expressed through Equation (6):

$$I_D = W \int_0^L J_p \cdot dl \quad (6)$$

where W , L and J_p are the channel width, the length of the drain contact and the flux of holes as the charge carriers, respectively. Table S3, Supporting Information, lists all the device parameters utilized in the simulations.

Concerning the influence of the distance C (see Figure 1b) between gate electrodes and interdigitated source and drain, one should notice that the double layers were formed at the gate electrode/electrolyte interface and at the semiconductor/electrolyte interface (situated above source–drain electrodes), as shown in Figure 2. Thus, the space between the gate electrode and the source–drain electrode remained electrically neutral and the potential in this region remains flat. Because there was no drop of the potential in this region, and the potential drops happened at the double layers at the interfaces, the parameter C was not expected to affect the device characteristics.

2.9. Gate Functionalization with DNA Probe Strands

For transistors functionalization, a procedure similar to the one described by Liu et al was employed.^[41] After the deposition of the OSC and assembly of the PMMA well, the gate electrodes were functionalized by putting a 100 μL drop of a PBS solution containing the anti-BPA ssDNA (concentration: 100 μM , to ensure the gate electrode surface saturation) inside the well. The OSC acted as a protection layer for the source and drain electrodes, preventing them from exposure to the thiolated DNA sequence. After 18 h of incubation, the devices were rinsed with a large quantity of pure PBS solution and then a drop of fresh PBS solution was put on their surface, to prevent direct exposure of DNA to air and also to remove any loosely bound DNA molecules from the gate.

2.10. Electrical Characterization of 2D-IJ EGOFETs Functionalized with DNA Probe Strands

The effects of functionalization on the transistors’ behavior were first evaluated by acquiring transfer characteristics after every functionalization step (i.e., “virgin” device, after ssDNA immobilization, after DNA hybridization).

The transistor’s response to the injection into the well of complementary DNA strands was evaluated by recording I_D and I_G currents as a function of time, while V_{GS} and V_{DS} were kept at constant values (-0.6 and -0.5 V , respectively). The

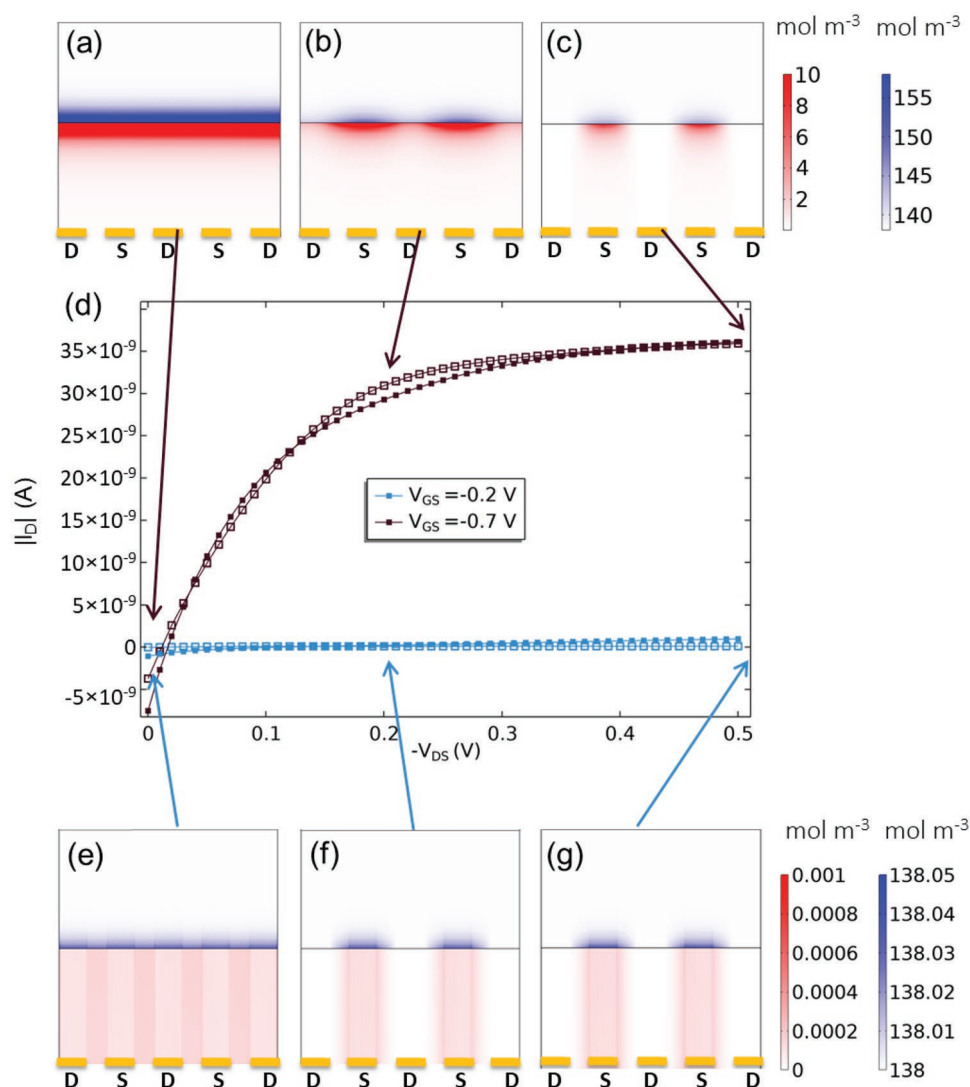


Figure 2. (a–c) and (e–g) Evolution of the charge carrier density (holes in red and anions in blue) at the electrolyte/OSC interface for different drain voltages $V_{DS} = 0, -0.2, -0.5$ V as indicated by arrows. Top and bottom panels ((a–c) and (e–g), respectively) correspond to two representative gate voltages $V_{GS} = -0.7$ and -0.2 V. For convenience, the output curves for $V_{GS} = -0.7$ and -0.2 V (the same as in Figure 2a) are shown in (d); experimental data are shown in dots and simulated data are in empty squares.

measurements duration was 4.380 s, currents were sampled every second. Current variations were measured in response to the injections of different solutions inside the electrolyte well: pure PBS, PBS containing the ssDNA, PBS containing the complementary DNA strand at the following molar concentrations: 10, 20, 40, 60, and 100 μM (with respect to the total liquid volume in the well).

3. Results and Discussion

3.1. Transistor Fabrication

Transistors were fabricated on Kapton polyimide foils. For the fabrication of the source, drain and gate electrodes, an inkjet-printable homemade suspension of gold nanoparticles was prepared. The formulation of this ink was recently published.^[37]

The semiconducting ink was prepared by dissolving the DPP–DTT powder in 1,2-dichlorobenzene. The rheological properties of the semiconducting ink were measured at room temperature. Surface tension was measured with a Kibron Aquapi tensiometer and exhibited a value of $33 \pm 1 \text{ mN m}^{-1}$; dynamic viscosity was measured with a Brookfield viscometer LVDV2T, it had a value of $11.35 \pm 0.04 \text{ cP}$ (at 24 rpm). Both values fall within the optimal range for printability required by our printing equipment.^[42]

The deposition of the electrodes was performed using a Dimatix Fujifilm DMP-2800 printer with 10 pL drops cartridges; the aforementioned homemade gold nanoparticle suspension was used. The final thickness of the printed electrodes was $\approx 300 \text{ nm}$ (estimated with a Dektak 150 mechanical profilometer) and their electrical resistivity at room temperature (measured with a Keithley 2601B System Source Meter in the four-probe configuration) was in the order of $10^{-7} \Omega \text{ m}$.

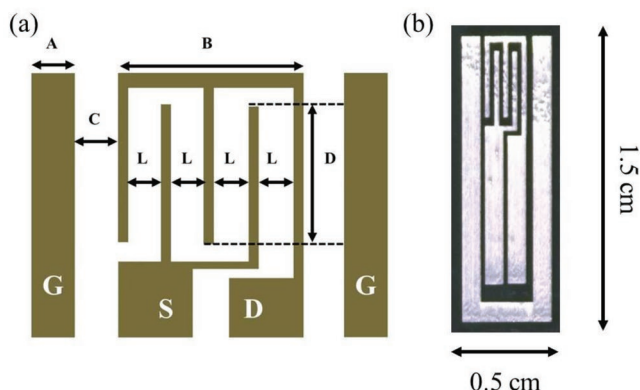


Figure 3. a) Scheme illustrating (not to scale) the transistors' active area nominal dimensions. $A = 1$ mm, $B = 2.25$ mm, $C = 0.375$ mm, $L = 0.2$ mm, $D = 4$ mm. b) Optical image of the inkjet-printed electrodes.

Figure 3a depicts a scheme illustrating (not to scale) the nominal dimensions of the transistors' active area; **Figure 3b** shows an optical image of the inkjet-printed electrodes.

As can be seen from **Figure 3**, the source and drain electrodes form an interdigitated comb (nominal channel width $W = 16$ mm, nominal channel length $L = 0.2$ mm, nominal $W/L = 80$ mm mm⁻¹). It should be noted that the gate electrode was designed and fabricated to completely surround the transistor's active area. Real dimensions were checked after deposition using an optical microscope (Olympus BX51, 20X magnification); an effective $W/L = 100 \pm 10$ mm mm⁻¹ was obtained.

Deposition of the OSC was performed either by drop casting (3D-DC and 2D-DC transistors) or by inkjet-printing (3D-IJ and 2D-IJ transistors); the aforementioned Dimatix printer was used in the latter case.

The wettability of the OSC ink on Kapton as well as on the printed gold layers has been investigated by static contact angle measurements (with Krüss Drop Shape Analyzer, model DSA25B). In both cases, we found very good spreading of the semi-conducting ink droplet over the surface (see **Figure S1**, Supporting Information). Contact angles using the sessile drop method have been measured in the range 5–10° on both materials, allowing us to evaluate the adhesion energy of the OSC at ≈ 65.5 mJ m⁻² (value obtained from the Young–Dupré equation).^[43] This value is consistent with the results reported elsewhere and describing similar materials.^[44]

It should be noted that for both drop cast and inkjet-printed devices, substrate treatments before and after the OSC deposition were the same; the OSC solution used in both cases was also the same (see Section 2).

Both drop-cast and inkjet-printed OSC layers exhibited thickness of a few micrometers (estimated with a Dektak 150 mechanical profilometer).

The device was then completed by glueing a polymethyl methacrylate (PMMA) well on the transistor's active area. Each well was obtained starting from a 5-mm thick PMMA film and was laser-engraved (total inner volume: 5 mm × 5 mm × 5 mm); it was glued on the Kapton substrate by means of double-sided adhesive tape. The purpose of the wells are twofold: on the one hand, it permits confining the electrolyte to the transistor's active area and on the other it reduces the water evaporation rate thus helping to keep the electrolyte concentration constant over time.

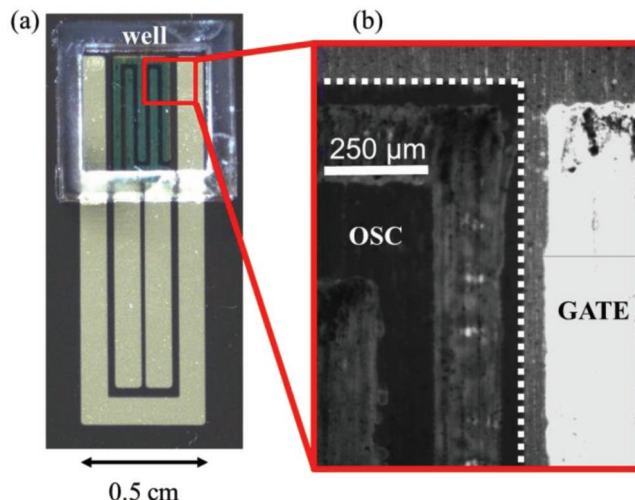


Figure 4. a) Optical image of an inkjet-printed EGOFET with a PMMA well mounted on the active area. The printed OSC is clearly visible as a green layer on the interdigitated source and drain electrodes. b) Optical image acquired with the printer's fiducial camera showing a detail between the transistor's channel and the gate electrode.

Finally, a drop of phosphate buffer saline (PBS) solution (100 μL) was deposited inside the PMMA well to completely cover the active area and part of the two branches of the gate electrode.

Figure 4a shows an optical image of an inkjet-printed, coplanar EGOFET with a PMMA well mounted on the active area. The printed OSC is clearly visible as a green layer on the interdigitated source and drain electrodes. **Figure 4b**, acquired with the printer's fiducial camera, shows a magnification of the gold gate electrode (whitish rectangle on the right) and the printed OSC (area within the dotted line).

3.2. Morphological Characterization

The morphology of printed layers was investigated by atomic force microscopy (AFM). **Figure 5a** shows a typical layer of DPP–DTT compared to the bare Kapton substrate. One can notice that the OSC forms a homogeneous film and that the typical features of the bare Kapton foil (scratches, wrinkles) vanish under the DPP–DTT layer. Due to the granular morphology of DPP–DTT, the surface roughness remains almost constant: 2 nm for bare Kapton versus 1.8 nm for DPP–DTT (root mean square values). **Figure 5b** shows the morphology of the printed gold layer before and after the deposition of DPP–DTT. Here also, a full coverage as well as a homogeneous organic film is obtained. All in all, we observe a smoothening of the surface by the OSC layer as the roughness values decrease from 43 nm for bare gold to 31 nm for DPP–DTT on top of gold.

3.3. Electrical Characterization

Figure 6 shows an example of output and transfer characteristics acquired on the four types of devices.

For the sake of clarity, the following **Table 2** summarizes the different types of devices that were fabricated and tested:

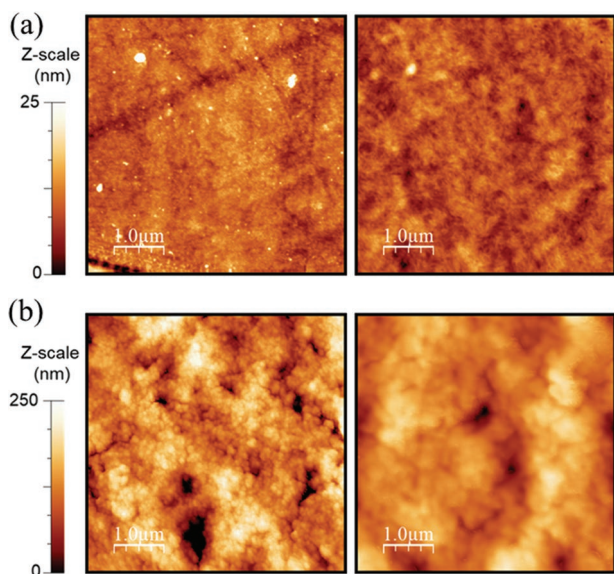


Figure 5. AFM images (scan size: $5\ \mu\text{m} \times 5\ \mu\text{m}$). a) Bare Kapton substrate (left); printed layer of DPP–DTT on Kapton (right). b) Printed gold on Kapton (left); printed DPP–DTT on gold (right).

As can be seen from Figure 6, in all cases devices show the typical p-type transistor behavior commonly reported for DPP–DTT transistors with gold source and drain contacts.^[45–47]

The extraction of the most important electrical parameters was performed by plotting the square root of the drain current I_D as a function of V_{GS} in the saturation regime and using Equation (7) to obtain a linear fit of the curve and calculate the values of the threshold voltage (V_{TH}) and the charge carriers mobility (μ);^[11,14] for the calculation of mobility, the actual W/L ratios (see Section 3.1) were used while the C_{TOT} value was measured by means of electrochemical impedance (data not shown) and corresponded to $\approx 1\ \mu\text{F cm}^{-2}$.

$$I_D = \frac{1}{2} \mu C_{TOT} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7)$$

The I_{ON}/I_{OFF} ratio was calculated by taking the maximum and minimum drain current values from the transfer curves plotted in logarithmic scale (see Figures S2 and S3, Supporting Information).

The following Table 1 presents the most important figures of merit for the four types of transistors, in the form mean value \pm standard deviation ($n \geq 3$ for each type of transistors).

Comparing the values reported in the table above, the following conclusions may be drawn:

1. The threshold voltage V_{TH} is almost identical in the four cases;
2. The charge carriers' mobility μ is slightly higher for the 3D-DC devices; this small difference (roughly a 2.7 factor) does not seem to depend on the transistors configuration (3D versus 2D) or on the OSC deposition technique (drop-casting versus inkjet-printing) as the other three types of devices show almost identical values;
3. The I_{ON}/I_{OFF} ratio is the same for the 3D-IJ, 2D-DC and 2D-IJ devices, the 3D-DC transistors showing again higher values.

This difference can be attributed to ON currents, which are higher in 3D-DC transistors ($\approx 10^{-7}$ A) than in the other types of devices ($\approx 10^{-8}$ A), the OFF currents being almost the same for the four kinds of transistors ($\approx 10^{-10}$ A).

The threshold voltage and charge carriers' mobility values of the four kinds of transistors described in this paper are perfectly comparable to those already reported for 3D EGOFETs where the same OSC (DPP–DTT) was deposited by spin-coating on thermally evaporated gold electrodes.^[13,47,48] On the other hand, our devices exhibit lower I_{ON}/I_{OFF} ratios (values $> 10^3$ are usually reported).^[13,47,48] This difference may be explained in terms of the lower I_{ON} currents (the OFF currents having the same orders of magnitude of similar devices reported in the literature) which can be attributed to the relatively small W/L that can be achieved with inkjet-printing.

3.4. Simulation of 2D-IJ Devices and Comparison to the Experiments

Herein, we will present and discuss the results of simulations of the 2D-IJ EGOFETs by bringing the device characteristics into focus. The output curve of the EGOFETs is obtained by sweeping the drain voltage V_{DS} at different given gate voltages and calculating the drain current as an output, whereas the transfer curve is obtained by sweeping the gate voltage V_{GS} for a given drain voltage and acquiring the current passing through the drain contact. Figure 7 depicts the output and transfer curves of the device where dots represent the experimental curves and empty squares represent simulated curves.

The simulated output and transfer curves show not only qualitative, but rather good quantitative agreement with the experimental ones. The linear and saturation phases of the output curves (respectively for V_{DS} up to approximately -0.1 V and from approximately -0.2 V) are clearly seen in Figure 7a. The output characteristics and the transfer curves of the device exhibit a pronounced feature that the transistor remains in the OFF state and practically does not respond to the changes in the gate voltage up to $V_{GS} = -0.4$ V. This feature is quantitatively reproduced by the simulations that showed that the OFF current regime and absence of the transistor action for low gate voltages is an electrostatic effect related to the device geometry. That is, the width of the organic semiconductor channel is too large such that low gate voltages cannot induce sufficient charge density at the electrolyte–organic semiconductor interface that would support the current flow.

It should be noted that there is a difference between the experimental and simulated transfer curves especially at high gate voltages. However, it is also noteworthy that there is even a difference between the corresponding data at the experimental output and transfer curves. That is, for the same gate and drain voltage values, drain currents in the transfer curve do not exactly match those of the output curve. This difference has been seen before in EGOFET devices and was related to the experimental way used to measure the currents in the output and transfer curves.^[36]

In the following, we focus on the concentration and potential profiles at the electrolyte–organic semiconductor interface, where the electric double layer is formed, outlining

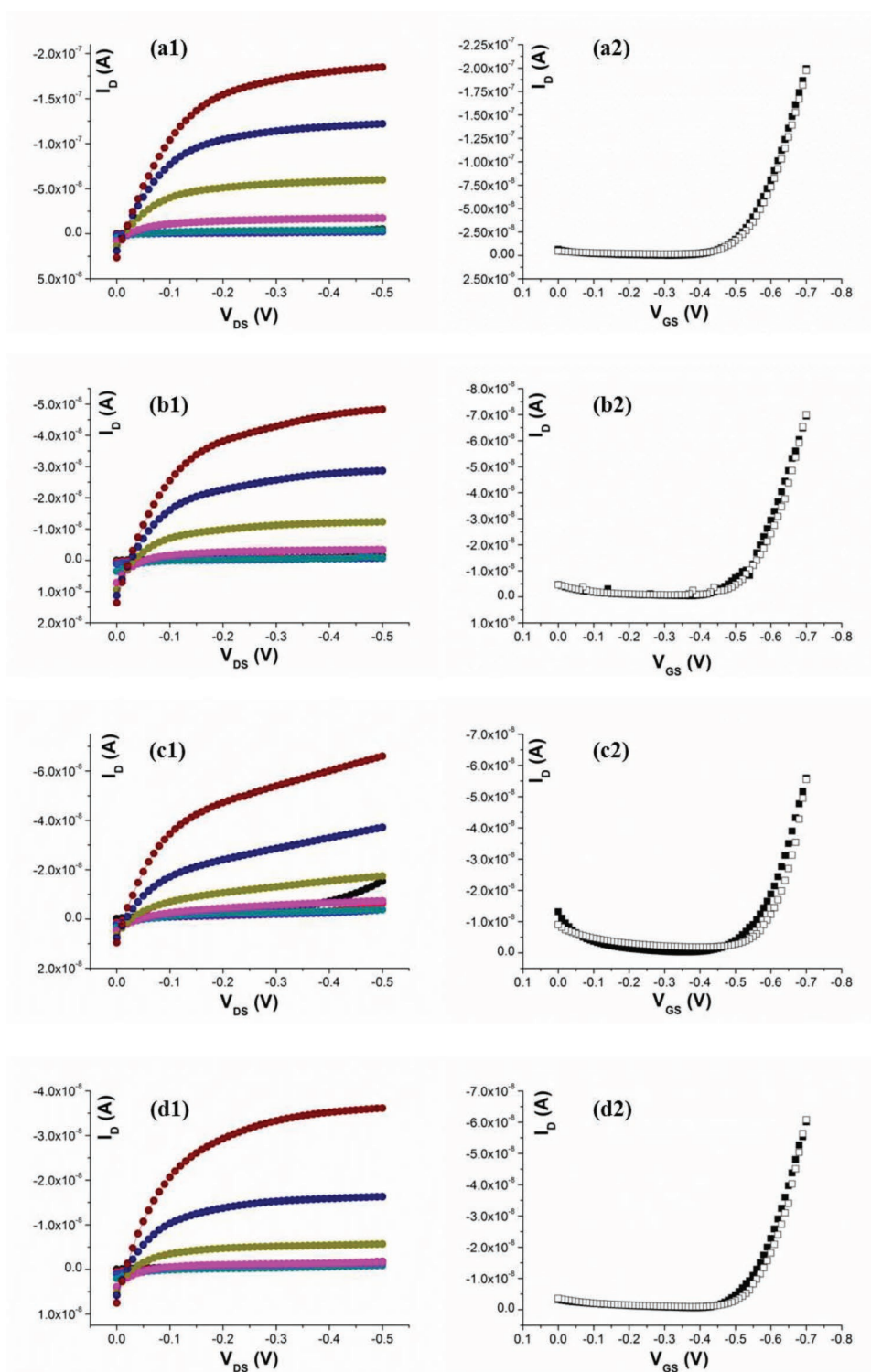


Figure 6. (Left) Examples of output characteristics for a1) 3D-DC, b1) 3D-IJ, c1) 2D-DC, and d1) 2D-IJ devices. For all curves: ● $V_{GS} = 0.0$ V, ● $V_{GS} = -0.1$ V, ● $V_{GS} = -0.2$ V, ● $V_{GS} = -0.3$ V, ● $V_{GS} = -0.4$ V, ● $V_{GS} = -0.5$ V, ● $V_{GS} = -0.6$ V, ● $V_{GS} = -0.7$ V. (Right) Examples of transfer characteristics for a2) 3D-DC, b2) 3D-IJ, c2) 2D-DC, and d2) 2D-IJ devices. For all curves: ■ forward curve, □ backward curve.

the difference between the standard operation of EGOFETs observed at higher negative voltages $|V_{GS}| > 0.4$ V and the off-current regime at lower voltages $|V_{GS}| < 0.4$ V. The operation of EGOFETs is relatively well understood:^[7,36,49] the application of

a negative voltage at the gate electrode changes the distribution of the ions within the electrolyte, such that positive ions come close to the gate, whereas negative ions accumulate close to the electrolyte/OSC boundary. The accumulation of the negative

Table 2. Summary of the four types of devices tested during our study.

Device code	Au wire as gate electrode	Inkjet-printed coplanar gate	Drop-cast OSC	Inkjet-printed OSC
3D-DC	●		●	
3D-IJ	●			●
2D-DC		●	●	
2D-IJ		●		●

ions at the interface induces accumulation of the holes on the other side of the boundary, in the organic semiconductor region. The upper panel in Figure 2 presents the evolution of the ions and holes concentrations at the electrolyte/OSC interface at $V_{GS} = -0.7$ V for three representative drain voltages corresponding to a linear regime ($V_{DS} = 0$ V), transition (pinch-off) regime ($V_{DS} = -0.2$ V), and a saturation regime ($V_{DS} = -0.5$ V). The corresponding ions and holes concentration profiles and electric field and potential distributions are shown in Figure S4, Supporting Information.

In the linear regime, when the drain voltage is low, holes are distributed homogeneously at the interface with the electrolyte (Figure 2a). As a result, the transistor operates in the ohmic regime when the current increases linearly with the drain voltage. With further increase of the magnitude of the drain voltage the charges start to deplete above the drain electrodes (Figure 2b), and the increase of $|V_{DS}|$ does not any longer contribute to the linear increase in the drain current. When $|V_{DS}|$ is further increased (Figure 2c), the device enters the saturation regime when the output current becomes constant. The saturation of the current is the result of two opposite trends: the growth of the depleted region above the drain electrode reducing the current and increase of drain voltage raising the drain current.

An evolution of the ions and holes concentration at the electrolyte/OSC interface for the case of the off-current regime ($V_{GS} = -0.2$ V) is presented on the lower panel of Figure 2. The corresponding ions and holes concentration profiles and electric field and potential distributions are shown in Figure S5, Supporting Information. For zero drain voltage the holes concentration at the interface is four orders of magnitude lower as compared to the case of $V_{GS} = -0.7$ V, see Figure 2e. As the result, the charges become completely depleted above the electrodes already at very low drain voltages ($V_{DS} = -0.2$ V see

Figure 2f,g and Figure S4, Supporting Information). This means that the transistor enters the saturation regime for gate voltages that are much lower than those corresponding to a typical EGOFET operation regime, and the current remains very low in the whole range of the device operation ($0 < |V_{DS}| < 0.5$ V). Note that the holes density at the electrolyte/OSC interface is low because in the present device the semiconducting layer is rather thick ($L_S = 1.5$ μm , see Figure 1). In the EGOFETs with thinner semiconductor layers, the holes density at the interface is much higher at low gate voltages, and therefore OFF current regime does not take place.^[36]

3.5. Complementary DNA Strand Detection

Such tests were performed only on the 2D-IJ devices.

An example of transfer curves acquired after each functionalization step is shown in Figure 8a.

It can be noticed that each functionalization step decreases the drain current values; since V_{TH} remains more or less constant throughout the whole functionalization process (calculated V_{TH} variations are always $<5\%$) this current variation may be attributed mostly to a decrease of C_{TOT} . This observation is not surprising and can be easily explained by considering the formation of an insulating DNA layer at the surface of the gate electrode.^[11,14] It should be noted that the transfer curves modification is actually a direct consequence of the gate functionalization as blank devices dipped in a pure PBS solution for the same amount of time did not show any significant modification of their transfer curves (data not shown).

Figure 8b depicts an example of response of a transistor functionalized with ssDNA probes to the injection of different concentrations of target DNA into the PMMA well. It can be observed that injection of pure PBS (arrow 1) or the same DNA probe strand already immobilized on the gate electrode (arrow 2) do not cause any significant variation of the drain current, but when the complementary DNA strand is injected (arrows 3 to 7) I_D decreases as a result of hybridization. Such a variation confirms the trend already observed on the transfer curves.

The reported example is far from being a fully optimized DNA sensor, it should be considered just as a proof-of-concept and, as such, extraction of significant figures of merit such as detection limit and sensitivity does not make much sense in

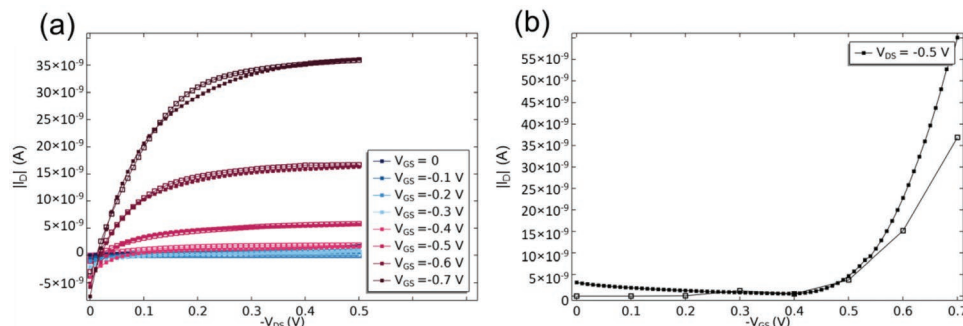


Figure 7. Calculated a) output curves and b) transfer curve of 2D-IJ EGOFETs for different gate voltages. Experimental data shown in dots and simulated data in empty squares.

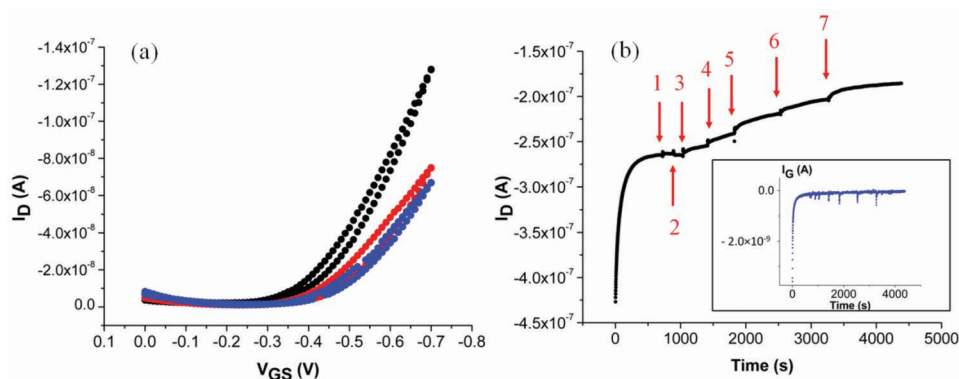


Figure 8. a) Transfer curves acquired on the same device (2D-IJ) at $V_{DS} = -0.5$ V. ● Virgin device, ● device after ss-DNA immobilization, ● device after hybridization. b) I_D current versus time ($V_{DS} = -0.5$ V, $V_{GS} = -0.6$ V) of a device whose gate electrode was functionalized with ss-DNA. The red arrows represent the moments where injections of different solutions inside the PMMA well occurred: 1) injection of pure PBS; 2) injection of PBS + SH-DNA; injections of complementary DNA strands at 3) 10 μM ; 4) 20 μM ; 5) 40 μM ; 6) 60 μM ; and 7) 100 μM . Inset: gate current recorded on the same transistor.

this context. These preliminary results, however, still represent an important achievement as they practically demonstrate that our 2D-IJ EGOFETs respond to charged molecules immobilized at the surface of the gate. These encouraging first results may potentially pave the way to the development of low-voltage sensors able to work in aqueous media.

4. Conclusions

In this paper, we reported for the first time a protocol for the fabrication of EGOFETs on flexible, plastic substrates by means of inkjet-printing. Four different types of devices were fabricated and characterized: transistors in a “classical” 3D configuration, transistors in a coplanar configuration and, for both types of devices, two diverse OSC deposition methods were employed, namely inkjet-printing and drop-casting. This choice allowed us to decouple the contribution of the devices’ geometry from that of the OSC deposition to the overall electrical behavior. All types of devices showed excellent electrical performances, comparable (in terms of threshold voltage and charge carriers’ mobility) to those of EGOFETs fabricated using costly and material-consuming techniques such as photolithography and spin-coating. Device operation was also modeled and analyzed using Nernst–Planck–Poisson equations describing, on equal footing, both the organic semiconductor and the electrolyte regions. The output and transfer curves were calculated, showing not only qualitative, but rather good quantitative agreement with the experiment. The charge and potential distribution inside the device were calculated and analyzed. In particular, it was shown that the “off-current” regime and the absence of the transistor action observed at low gate voltages $|V_{GS}| < 0.4$ V is an electrostatic effect related to the device geometry. Finally, to practically demonstrate a perspective application of the all-printed devices, the coplanar gate was functionalized with single-stranded DNA and the transistors were successfully used for the detection of the complementary DNA strand in a liquid medium. The results presented in this paper are twofold: i) they may open an avenue to the development of a new generation of low-cost, low-power, and flexible circuits and sensors ii) they also demonstrate that Nernst–Planck–Poisson modeling

represents a powerful tool allowing quantitative device design, modelling, and analysis.

The next steps of our work will be the utilization of the model described herein to predict the transistors’ electrical behavior as a function of the materials and geometry employed for their fabrication, and the modification of said model to take into account surface functionalization strategies similar to that described in Sections 2 and 3.5. This will be the object of forthcoming papers.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was funded by the French National Research Agency (Agence Nationale de la Recherche) through the project EGOFLEX ANR-17-CE08-0025, and by the Swedish Research Council (Project 2017–04474). The computations were performed on resources provided by the Swedish National Infrastructure for Computing (SNIC) at NSC and HPC2N.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

biodetection, electrolyte-gated field-effect transistors, inkjet-printing, finite element modeling, Nernst–Planck–Poisson equations

Received: February 25, 2022

Revised: July 1, 2022

Published online:

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