High speed universal NAND gate based on weakly coupled RF MEMS resonators

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Abstract

Logical gates have been used in implementation of logic sequential and combinational circuits especially in computers, DSPs and microprocessors. They are mostly fabricated based on CMOS technology that provides a few nano-seconds of delay for each digital gate. Due to limitations in more scaling CMOS transistors and cause of short channel effects, some engineers and researchers believe that there is a huge demand for new devices and fabrication technologies to produce faster logic gates. In this paper, a new architecture for NAND gate is presented which operates based on mechanical resonance of a network of weakly coupled resonators that resonate in radio frequencies. This design is achieved by employing the associative memory property of Hopfield neural networks and the theory of weakly coupled resonators. The main advantage of the proposed design is in its capability to reach out delay times of the order of 1 nano-seconds or even less. One solution to decrease the delay time can be increasing the resonance frequency of resonators which are processing elements of resonators network. In this paper just the new idea of implementation NAND gate based on weakly coupled RF MEMS resonators is presented and evaluated. Other criteria like gate power consumption, effects of temperature,

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fan in, fan out and noise margin are not discussed. Regarding the rapid growth in MEMS technology, resonators with Super High Frequency (SHF 3-30 GHz) are now available and those with Extremely High frequency (EHF 30-300 GHz) will soon be in market which enables the presented design to achieve higher speeds. In addition, mechanical resonators are more fault tolerant than CMOS circuits when utilized in harsh environments which exposed to ionic beams or electron beam radiations. In space applications, the satellite and payload are exposed to huge bombardments of space electrons and ions beams. So, the proposed NAND gate can be a good solution for enhancing reliability of devices and systems exposed to space radiations.

Keywords: Weakly coupled resonators, Hopfield neural networks, Universal NAND gate design, RF MEMS resonators, Mechanical neuroprocessing.

1. Introduction

In recent decades, we have witnessed the inevitable slowdown of Moore's law and lots of analysts have predicted that the era of exponential gains in microelectronic is coming to an end [1]. Various ideas are being developed to be introduced as alternative approaches for computation like quantum computing [2] and neuromorphic computing [3, 4]. Also, brain inspired electronics such as memresistive [5, 6] and oscillator based [7, 8, 9] systems are growing rapidly in recent years and brings up a competitive field for beyond Moore computation.

Oscillator based systems use the highly complex dynamics of coupled oscillators for computation. The genuine idea returns back to 1950s [10, 11, 12] but is currently an active area of research and shows utility for certain types of challenges such as image processing [13] and optimization problems (energy minimizing)[14]. This type of computing basically occurs by oscillators interactions, specifically their synchronization that is affected by the interconnection of the oscillators. Oscillator based systems can carry information based on both phase and frequency oscillatory signals. In Phase based systems, oscillators operate at almost the same frequency and information is represented through

phase.

As mentioned, one ground setting capable of forming a hardware basis for neurocomputing is a network of oscillators. Hoppensteadt and Izhikevich proved that a network of properly connected oscillators can perform associative memory operation regardless of the physical nature of the oscillators [15, 16, 17]. Various attempts with oscillators of different kinds have been subject to research in order to establish a ground structure to perform specific tasks. Many types of oscillators can realize the role of neuron function. Structures with oscillatory neurons of magnetic spin-torque [18, 19, 20],oxide-based [21], CMOS ring [22], injection locking [23] optical laser-based oscillators [24], superconducting Josephson junctions [25, 26] and micro or nano-electro-mechanical systems [27, 28, 29, 30, 31, 32, 33, 34] have been proposed. Several of these works are seeking a platform for pattern recognition, making use of the associative recall property presented by coupled oscillators array. Oscillator based systems are also presented in cryptography [35], pattern generation and gait control [36, 37]. In another research, an energy efficient integrated MEMS neural network was fabricated for sensing and computing simultaneously [38].

This work focuses on Radio Frequency Micro-Electro-Mechanical Systems (RF MEMS) as oscillatory neurons. MEMS oscillators are among the most widely used systems in ubiquitous areas such as sensing, biomedical implants and wireless communications. RF MEMS oscillators are high frequency resonant systems that play an important role in the field of telecommunications. Lately, much attention has been drawn to these systems in order to be utilized in the area of Generation 5 (5G) wireless networks. Operating resonant frequency in such systems can reach up to multiple GHz. Various resonators with different transduction mechanisms exist with utilities in commerce from the early 1.156 GHz disk resonator presented in [39] to the late Super High Frequency(SHF) resonators with up to 30 GHz working frequency [40]. Micro/Nano electromechanical systems (MEMS/NEMS) could provide new solutions for computing and memory systems. Ultra low power consumption, compatibility and reconfigurability are some advantages of MEMS/NEMS memory systems in comparison

with MOSFET technology [41].

The main intention of the present work is to design a structure based on oscillatory network to be a basis for phase logic computing. This is done by employing RF MEMS oscillators as neurons which are electrically interconnected constituting the network. This architecture is intended to perform as a NAND logic gate. The mentioned gate is working on a basis of mechanical resonators, so we can call this as electromechanical neurocomputers. The structure presented in this paper may possibly be an alternative solution for prevailing CMOS based NAND gates in some applications due to its high speed and the fact that the RF MEMS technology is growing rapidly and yet has a long way to grow up. In order to apply the proposed microelectromechanical gate in real world applications, it is essential to add more parts considering other criteria like power consumption, noise margine and fan out which are not discussed in this paper.

In the following sections, first we are going to define weak coupling in an array of resonators and the conditions in which the Andronov-Hopf bifurcation occurs. This specific critical regime is vital for the resonators to have sustained constant amplitude oscillations. Next, in section III we present a structure of resonators arranged to form a Hopfield neural network. Section IV, proposes the main goal of this work that is to design a NAND logic gate and the method that led to this particular design. Simulated results come in the next section and are analyzed. Finally, we sum up the work done in this paper in the conclusion.

2. Theory

2.1. Weakly Connected RF MEMS Resonators

Studies on neurophysiology illustrate the existence of synaptic connections in brain circuitry and among tens of billions of excitatory and inhibitory neurons. Action potentials or spikes, believed to be chemical-based electrical pulses, generated by the excitatory neurons while excite the inhibitory cells and they are inhibited in reciprocation. This action of excitation, also known as firing, forms dynamic synaptic connections in brain.

Different models have been proposed to mimic this dynamic connectivity and neuronal behavior existing in the nervous system. For instance, comprehensive models such as Hodgkin-Huxley, empirical models like Mc'Cluch-Pitts and Hopfield's network and canonical models including the voltage Controlled Oscillator Neuron(VCON) are among the many models constituting the literature in mathematical neuroscience[42].

Experimental observations have revealed that in case of spikes accumulation (integration) in a particular neuron (caused by other neurons via synapses) the neuronal activity of that neuron can exceed a certain threshold which leads to firing repetitive spikes, otherwise the neuron remains quiescent. A different approach for describing neuronal activity consists of replacement of neurons with periodic oscillators, where the phase of each oscillator plays the role of spike time. This rhythmic or oscillatory dynamical behavior is also observed in various brain parts, including olfactory bulb, thalamus, neocortex and hippocampus[43].

Inspired by biological systems and making use of the rhythmic analogy of physical artificial oscillators and biological neurons one can present an oscillator based model. Here we essentially consider an especial category of Weakly Connected Oscillatory Networks(WCONs) which are capable of information processing and pattern recognition using their proposing associative memory property [17]. Dynamics of such a system with n oscillatory neurons of dynamical order m can be described as follows using the Malkin's theorem [44]:

$$\dot{x_i} = f_i(x_i) + \epsilon \sum_{j=1}^{n} g_{ij}(x_i, x_j, \epsilon) \tag{1}$$

Where each of vectors $x_i \in \mathbf{R^m}$ shows activity of $i'th$ oscillator, function $f_i : \mathbf{R^m} \to \mathbf{R^m}$ describes its internal dynamics function, $g_{ij} : \mathbf{R^{mxn}} \to \mathbf{R^n}$ defines the coupling among the units and $\epsilon \ll 1$ is a small parameter that guarantees a weak connection among the cells.

Eq. (1) defines dynamics of a general case of arbitrary weakly coupled oscillators in a network of oscillators, however this paper focus on a specific type of mechanical oscillator as mentioned earlier, the RF MEMS oscillators. A network

of n coupled mechanical oscillators is described as follows:

$$m\ddot{x_i} + f(x_i)\dot{x_i} + g(x_i) = \sum_{j=1}^{n} (p_{ij}\dot{x_j} + k_{ij}x_j) \tag{2}$$

Where x_i shows each oscillator's resonant body's displacement with respect to a determined reference position, m describes its effective mass and f and g are damping and stiffness functions, respectively. Right hand side of the equation reveals the effect of connections in the network in which p_{ij} and k_{ij} show the strength of electrical and mechanical connections (conductance and mechanical spring constants) between i^{th} and j^{th} oscillators.

Employing complex change of variable $z_i = \dot{x_i} + i\omega x_i$ wherein $\omega = \sqrt{\frac{k}{m}}$ is resonance frequency of the dynamic system, we can achieve the canonical dynamic model of the network as follows:

$$\dot{z_i} = (c + i\omega)z_i + (a + ib)z_i|z_i|^2 + \sum_{j=1}^{n} c_{ij}z_j \tag{3}$$

where:

$$c_{ij} = \frac{1}{2m}p_{ij} - \frac{i}{2m\omega}k_{ij} \tag{4}$$

and parameters a, b and c are as follows:

$$\begin{aligned} a &= -\frac{f''_{xx}}{16m\omega^2} \\ b &= \frac{3mg''' - 2(f'_x)^2}{48m^2\omega^3} \\ c &= -\frac{f'_\lambda}{2m}(\lambda - \lambda_H) \end{aligned}$$

Note that forms of the functions f and g depend on geometry, properties of material, features of the feedback loop and other characteristics of the oscillator, however particular forms of these functions do not affect the normal form (3), but only the parameters a, b and c. For more detailed analysis, see [27] and [44].

In order to have sustained constant amplitude oscillations, the super-critical Andronov-Hopf bifurcation must occur and this is guaranteed when $a < 0$ and

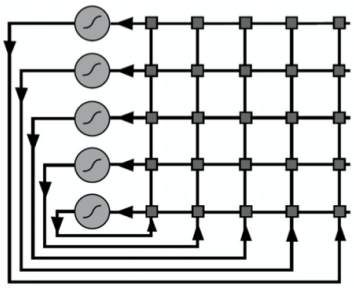

Figure 1: MEMS Oscillator Neural Network

c increases through the value 0. As mentioned earlier, parameters a, b and c are calculated based on the characteristics of the oscillator, including, damping and stiffness functions (and their derivatives f', f'' and g'''), effective mass m and the frequency of the dynamical system ω. Here, the damping function f is considered to be the Van der Pol damping, $f(x, \lambda) = x^2 - \lambda$ where parameter λ is proportional to the bias voltage applied to the oscillator and λ_H is the threshold value for damping sign, here is assumed to be $\lambda_H = 0$. Also, stiffness function is modeled by Duffing stiffness $g(x) = x + x^3$ that is trivial to be an odd function. For detailed analysis see [27].

2.2. Associative Memory Using Oscillatory RF MEMS Network

As said earlier, a network of oscillators interconnected suitably has autocorrelative associative memory similar to the one present in Hopfield neural networks. In oscillatory networks each pattern is stored in a synchronized phase relation that fluctuates with the corresponding limit cycle. It is proved for presenting associative memory property, it is vital that all the oscillators operate at same frequency. Also, in this particular work in which RF MEMS oscillators are being used, the mechanical interactions between the cells must be negligible and the electrical interactions must be symmetrical i.e. $k_{ij} = k_{ji} = 0$ and $p_{ij} = p_{ji}$. In case of the mentioned conditions, the network always converges to an oscillatory phase-locked pattern. There could be many such phase-locked patterns corresponding to many memorized patterns. The proof and detailed

analysis can be found in [17], [27].

Figure 1 shows a MEMS oscillatory network having 5 MEMS resonators fully interconnected. This is a schema of the network we are talking about here in which there is an electrical connection between every couple of resonators that ought to be symmetric. The question that raises here is that how the strength of each of these connection is determined? The answer can be found in the patterns that the network stores. In other words, sets of information (in the form of vector patterns) which are intended to be memorized by being coded to oscillator's phase relations determine the connection values of the network.

Among the many possible learning algorithms that were published [45], [46],[47] here we employ the Hebbian learning algorithm to design the synaptic weights (electrical connections) which, as stated, are realized by the externally connecting signals.

Suppose set of "m" complex vectors are given to be memorized by the network:

$$\xi^k = (\xi_1^k, \xi_2^k, ..., \xi_n^k); \quad |\xi_i^k| = 1 \qquad \mathrm{k} = 0, ..., \mathrm{m} \tag{5}$$

Where ξ^k is complex vector and ξ_i^k is i_{th} element of ξ^k vector.Connection weights Matrix can be obtained using the Hebbian learning rule as follows:

$$c_{ij} = \frac{1}{n} \sum_{k=0}^{m} \xi_i^k \bar{\xi}_j^k \tag{6}$$

Where n is the number of network cells and c_{ij} determines the corresponding weight between i^{th} and j^{th} neurons.

Now that the ability of the oscillatory networks to perform associative memory operation is defined and clarified, we are going to make use of this property and design a logic gate based on association of the logic states. In the next section, first some preliminaries to the subject will be introduced then the proposed gate architecture is presented.

3. MEMS Based NAND Gate

The main goal of this work is to benefit from the auto associative memory property of the weakly coupled oscillators network in order to propose an idea for NAND logic gate implementation. This section is mainly concerned with this gate, the characteristics and the path to the established architecture.

Figure 2 shows the network architecture that is the basis for the NAND logic gate. The network consists of 8 RF MEMS resonators connected electrically as shown. Outputs 5 and 8 of resonators determine the gate's output logic. Whenever the two outputs synchronize in-phase, gate's output is considered as logic 1. Otherwise, when they synchronize anti-phase, gate's output reveals logic 0 that will be discussed further.

Our intention of designing the universal NAND logic gate is due to the fact that NAND gates are universal gate which means any other Boolean function can be implemented only using a combination of this type of gate. Hence, owning a NAND gate designed by this particular computation paradigm means having access to any other logic gate needed for logic operation.

Current structure, Fig. 2, is achieved by a series of trials and errors through an exhaustive search in networks with different number of neurons having different learning patterns and different couple of cells as the gate's output. This search started with a network of 4 RF MEMS oscillators weakly connected. Having tried all the possible combinations of the 4 dimensional vectors as learning patterns and couple neurons as the output of the gate, no plausible result has been gained. The search continued, this time in a space of 8 neurons structure, passing through the same route, the architecture of Fig. 2 is achieved. As depicted in Fig. 2 outputs of the cells 5 and 8 could generate acceptable logical outputs which can be considered as output of the NAND gate.

This oscillatory neural network ought to have the capability to correctly retrieve all the logic states of NAND gate compatible with the 8-cells structure presented here. These compatible states are in fact the corresponding logic states of the truth table (Table 1) that are shown in Table 2. As is indicated,

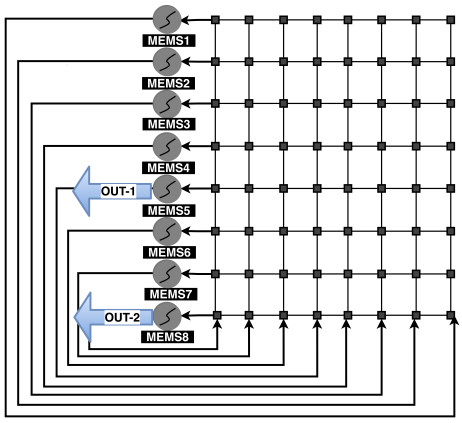

Figure 2: MEMS oscillatory network based NAND Gate

total number of 16 modified states constitute all the logical states that are in fact input to the designed NAND gate as patterns. The gate must be able to match correctly all states with their intended logic shown under the column T of the Table 2. In order to match all the 16 states with their true logic values as mentioned earlier the network must be trained correctly that means to adopt the right set of patterns, among all possible, for the network to learn and adjust the synaptic connection weights.

Since the neurons of the proposed NAND gate are oscillators, concept of logic output of the NAND gate must be clarified. For this reason, unit of data(bit) is re-established. As mentioned earlier, the information is coded in the network's oscillatory neurons phase relations, either in-phase or anti-phase synchronizations. Thus, the phase relation between every two oscillatory neurons determines a new bit (binary digit) used as unit of data. This unit of data is logic 1 in case of in-phase oscillations and logic 0 in case of anti-phase oscillations of the neurons. This idea is essentially similar to the one presented in Parametrons in 1950s [12]. In other words, two binary states (bits of 0 or 1) are determined by phase difference of oscillators which in a synchronization situation can be 0 or π. We call this idea *phaselogic*. Different logical gate operations were implemented in Parametrons using classical RLC circuits as os-

cillators. Recently, new interest is found in utilizing the phase logic approach in computing devices at nanoscale, using electromechanical nano-oscillators [48], super conducting nano-oscillators [49] or relaxation nano-oscillators [50].

Flowchart of Fig. 3 shows the algorithm that led to the NAND gate design. This flowchart describes the exhaustive search procedure which starts with determining the number of the cells in network. Beginning with 4 cells as stated earlier this structure isn't capable of establishing the desired NAND gate. The algorithm continues by adopting 8 cells for the network then a set of 5 patterns is selected and the network is trained based on Hebbian learning rule and the algorithm checks if any couple of neurons can play the role of gates output correctly. This means that some sets of patterns similar to all 16 logical patterns of the Table 2 are imposed on the network as inputs and checked if they are fully generating the true values in the NAND output based on the phaselogic. The algorithm goes on and try all combinations of oscillators as outputs and all combinations of patterns as training set till it finds a specific combination to satisfy all the input/output relations. This specific design is shown in the Figure 2 with cells number 5 and number 8 as defined outputs. Hence, here we employ the phase logic in order to determine the gate's logical output. The in-phase oscillations of the cells 5 and 8 specify logic 1 or $True$ value and the anti-phase oscillations specify logic 0 or $False$ value in the NAND gate's output.

As is stated, phaselogic also suggests some information about the network oscillators' phase relations. For instance, input pattern [1 0 0 1 0 1 1 0] shows that oscillators 1, 4, 6 and 7 are operating in-phase with respect to each other and anti-phase with respect to rest of the oscillators.

It must be noted that the dynamics of the proposed network of Fig. 2 is described by the canonical model presented in eq. (3) with number of cells $n = 8$. In fact, system of 8 ordinary differential equations with 8 complex variables, $z_1, z_2, ..., z_8$, defines the dynamics of this logic gate. Input patterns to NAND gate are in fact initial values to this system of ODEs and the response to this system of ODEs determines the network's outputs. The system of ODEs

Table 1: NAND logic truth table

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

are as follows:

$$\begin{aligned}
\dot{z_1} &= (c+i\omega)z_1 + (a+ib)z_1|z_1|^2 + C_1 \\
\dot{z_2} &= (c+i\omega)z_2 + (a+ib)z_2|z_2|^2 + C_2 \\
\dot{z_3} &= (c+i\omega)z_3 + (a+ib)z_3|z_3|^2 + C_3 \\
\dot{z_4} &= (c+i\omega)z_4 + (a+ib)z_4|z_4|^2 + C_4 \\
\dot{z_5} &= (c+i\omega)z_5 + (a+ib)z_5|z_5|^2 + C_5 \\
\dot{z_6} &= (c+i\omega)z_6 + (a+ib)z_6|z_6|^2 + C_6 \\
\dot{z_7} &= (c+i\omega)z_7 + (a+ib)z_7|z_7|^2 + C_7 \\
\dot{z_8} &= (c+i\omega)z_8 + (a+ib)z_8|z_8|^2 + C_8
\end{aligned} \tag{7}$$

Where:

$$C_i = \sum_{j=1}^{8} w_{ij} z_j \tag{8}$$

Having presented the structure of designed NAND logic gate now we are ready to impose the input patterns corresponding to the possible logical states and present the simulated results.

4. Simulations and Results

In order to validate the claimed capability of the proposed neural network, we simulated the network response to all 16 patterns of the Table 2, which are all states possible for the 8-cells structure, to see if the network can produce the logical outputs correspond to all inputs. To avoid repetition, here we present one out of every four patterns corresponding to each logical state for X and Y.

Table 2: NAND logic input patterns

X, Y	Z_0	T
	[1 0 0 1 0 1 1 0]	T = 1
X = 0	[1 0 0 1 1 0 0 1]	
Y = 0	[0 1 1 0 0 1 1 0]	
	[0 1 1 0 1 0 0 1]	
	[0 0 1 1 0 1 1 0]	T = 1
X = 1	[0 0 1 1 1 0 0 1]	
Y = 0	[1 1 0 0 0 1 1 0]	
	[1 1 0 0 1 0 0 1]	
	[1 0 0 1 0 0 0 0]	T = 1
X = 0	[1 0 0 1 1 1 1 1]	
Y = 1	[0 1 1 0 0 0 0 0]	
	[0 1 1 0 1 1 1 1]	
	[1 1 0 0 0 0 1 1]	T = 0
X = 1	[1 1 0 0 1 1 0 0]	
Y = 1	[0 0 1 1 0 0 1 1]	
	[0 0 1 1 1 1 0 0]	

The first 12 logical patterns that represent the logic states $X = 0, Y = 0$ and $X = 1, Y = 0$ and $X = 0, Y = 1$ are expected to produce in-phase resonances in gate output which implies that the gate output is logic 1. The remaining four input patterns corresponding to the state $X = 1, Y = 1$ must show anti-phase resonances in their dynamic response so that logic 0 is determined in the NAND gate output. Among sixteen inputs noted in Table 2, the simulations result for input logical patterns Z1 = [1 0 0 1 0 1 1 0], Z5 = [0 0 1 1 0 1 1 0], Z9 = [1 0 0 1 0 0 0 0] and Z14 = [1 1 0 0 1 1 0 0] are depicted as follows:

The patterns depicted in Fig. 4 to Fig. 7 show the initial and final stages of the association process. In other words, the left hand side pattern shows the initial state or input pattern that is in fact one of the logical states of the

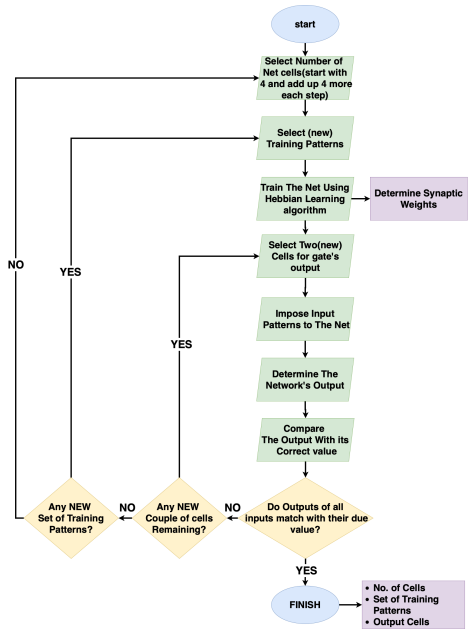

Figure 3: NAND gate design algorithm

Table 2. The dots in the middle part shows the process of fluctuations which leads to the pattern association or regeneration. Actually this is some periods of oscillation time that network takes to synchronize. The right hand side pattern is the final or output pattern.

As depicted in the patterns of Fig. 4 to Fig. 7, the cells number 5 and number 8 are considered as the NAND gate's output. It is shown that in-phase synchronization of these two neurons corresponds to logical output 1, as shown in Fig. 4, Fig. 5 and Fig. 6 and anti-phase synchronization of the mentioned resonators corresponds to logical output 0, as can be seen in Fig. 7.

Fig. 8 shows the oscillatory response of the network to the input pattern [1 0 0 1 0 1 1 0] which is one of the four patterns equivalent to logic input $X = 0, Y = 0$. The two neurons defining the NAND gate output (namely MEMS-5 and MEMS-8) are oscillating in-phase. Hence, the mentioned input pattern corresponds to logic 1 as is expected.

Fig. 9 shows the oscillatory response of the gate designated outputs to the

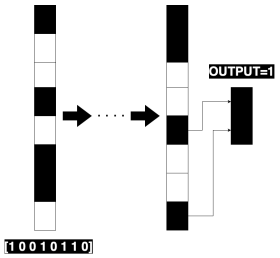

Figure 4: Regeneration of pattern Z1 = [1 0 0 1 0 1 1 0]

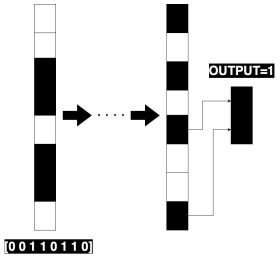

Figure 5: Regeneration of pattern Z5 = [0 0 1 1 0 1 1 0]

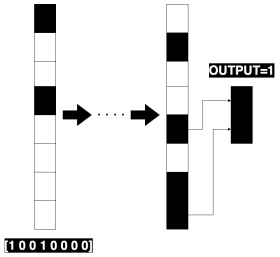

Figure 6: Regeneration of pattern Z9 = [1 0 0 1 0 0 0 0]

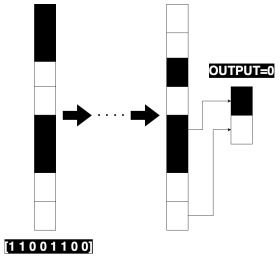

Figure 7: Regeneration of pattern Z14 = [1 1 0 0 1 1 0 0]

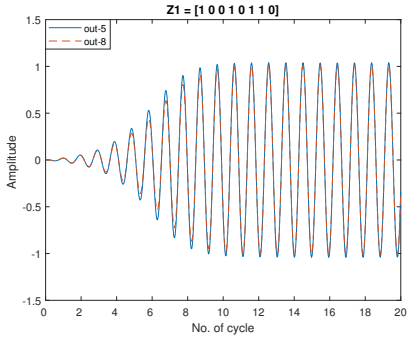

Figure 8: Gate response corresponding to input pattern Z1 = [1 0 0 1 0 1 1 0], X=0 , Y=0 , Output = 1

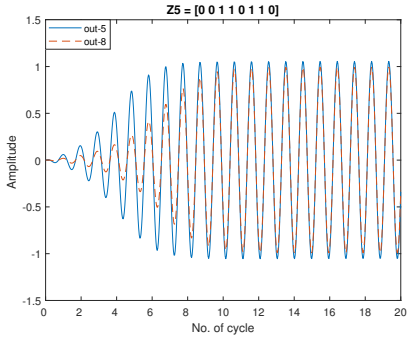

Figure 9: Gate response corresponding to input pattern Z5 = [0 0 1 1 0 1 1 0], X=1 , Y=0 , Output = 1

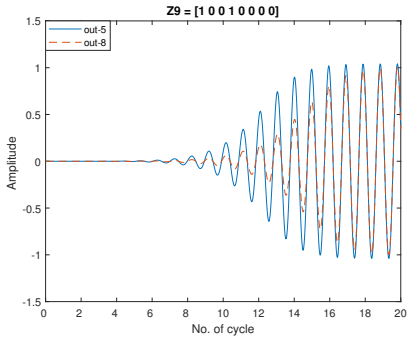

Figure 10: Gate response corresponding to input pattern Z9 = [1 0 0 1 0 0 0 0], X=0 , Y=1 , Output = 1

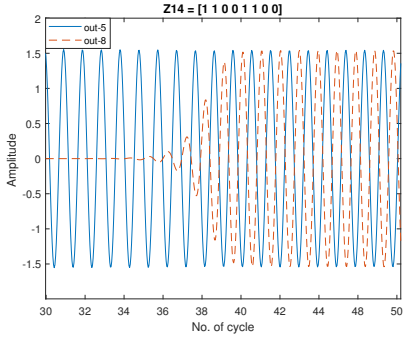

Figure 11: Gate response corresponding to input pattern Z14 = [1 1 0 0 1 1 0 0], X=1 , Y=1 , Output = 0

input pattern [0 0 1 1 0 1 1 0] that is one of the four states equivalent to $X = 1, Y = 0$. As expected, the response is in-phase i.e. logic 1.

Figures 10 and 11 show the responses to the input patterns [1 0 0 1 0 0 0 0] and [1 1 0 0 1 1 0 0], respectively. The former is one out of the four logic patterns of the state in which $X = 0, Y = 1$ and the later represents a logic pattern among the four of the state $X = 1, Y = 1$. As illustrated, Fig. 10 shows in-phase oscillations so that the NAND gate output is logic 1. But, in Fig. 11 anti-phase outputs can be seen which shows output logic 0.

Table 3 shows the number of cycles that the output neurons (MEMS-5 and MEMS-8) need in order to synchronize, either in-phase or anti-phase, subjected to different input patterns. Based on simulation results the maximum number of cycles needed for the output oscillators is revealed to be 39. This number specifies the maximum delay time of the proposed NAND gate to produce the output. Using the super high frequency RF MEMS resonator with 45GHz operating frequency the gates delay time can be calculated as follows:

$$t_d = 39 \times \frac{1}{45 \times 10^9} \approx 0.86ns$$

As can be seen in Table 3, in most of the cases the resonators produce gate output in less than 10 period times. If resonance frequency is assumed to be 45 GHz, then the delay time will be less than 222 ps for ten cycles to generate the output. But, for the last four input cases in Table 3, it needs more than 23

Table 3: Number of cycles to synchronize for different inputs states

Logicinputs	Cycles to generate output	Logic output
[1 0 0 1 0 1 1 0]	7	
[1 0 0 1 1 0 0 1]	2	T = 1
[0 1 1 0 0 1 1 0]	8	
[0 1 1 0 1 0 0 1]	2	
[0 0 1 1 0 1 1 0]	9	
[0 0 1 1 1 0 0 1]	2	T = 1
[1 1 0 0 0 1 1 0]	10	
[1 1 0 0 1 0 0 1]	9	
[1 0 0 1 0 0 0 0]	18	
[1 0 0 1 1 1 1 1]	2	T = 1
[0 1 1 0 0 0 0 0]	9	
[0 1 1 0 1 1 1 1]	1	
[1 1 0 0 0 0 1 1]	23	
[1 1 0 0 1 1 0 0]	**39**	T = 0
[0 0 1 1 0 0 1 1]	23	
[0 0 1 1 1 1 0 0]	24	

periods to produces proper output which is more than 0.5 ns. For input case $Z14$, the worst case, the most delay occurs which is 39 period times. Due to Fig. 11 the anti-phase outputs can be seen in after passing 12 periods but the amplitude of MEMS-8 needs more time to reach the desired level. It should be noted that delay time is inversly related to resonant frequency. In the other side, in TTL technology, for two-input NAND gate, CD74HCT00, the maximum delay time is 30ns. There are some other CMOS NAND gates which have usually larger delay time than 30ns (for two-inputs high speed CMOS NAND logic gate, 74HC03, the maximum delay is 150ns).

As another advantage of proposed NAND gate, it is more reliable than CMOS devices when exposed to ion or electron beams radiations. One ma-

jor problem of CMOS devices in space applications is vulnerability to space radiations. Huge amounts of charged beams can penetrate the shields and materials and enter active regions of CMOS devices. Some of the charges may be bypassed by some specific metallic paths or mechanisms but, some of them accumulates in some regions and would make problems by passing time. Accumulated charges on surfaces and silicon oxide interfaces cause threshold voltage drift and changing quiescent point of transistors which may cause catastrophic faults. Also, penetration charged ions and electrons to solid state devices would destroy uniform crystal structure of atoms and cause many point defects in solid state bulk region. These point defects can cause leakage and latch up of CMOS circuits which ends up to catastrophic faults or device burn out.

In the presented universal NAND gate, RF MEMS resonators produce sinusoidal signals by mechanical resonance in radio frequencies. In case charged particles bombardment, penetrating charged ions or electrons to resonant mechanical structures would not affect the resonance frequency. So, it is more reliable than CMOS devices which may be degraded by accumulated charges on surfaces and dielectrics. In case of exposing to electron and ion beams, charge accumulation and point defects in crystal structure would not affect catastrophically the resonant frequency and amplitude of the signals in mechanical neurocomputers.

5. Conclusion

During past decades CMOS has been dominant technology in fabrication of digital devices. There has been a permanent demand to increase the speed of logical circuits and reduce the delay in logic gates. Now, the minimum feature size in CMOS technology is in order of a few nanometer and it is more difficult than before to continue scaling down the dimensions of devices. Other substrate materials and other processing techniques are investigated in order to provide logic gates and processors with less delays. In this paper a new idea for NAND gate architecture is proposed in which a network of weakly coupled RF MEMS

resonators can produce the gate output in less than 1 ns. It consists eight RF MEMS resonators which are connected to each other based on Hopfield neural networks structure. Each input-output configuration is considered as a pattern which should be memorized by trained Hopfield neural network. In other words, eight weakly coupled RF MEMS resonators perform as eight neurons Hopfield neural network which should be trained as an associative memory which regenerates proper output in accordance to different inputs. In this paper finding network weights was demonstrated in a flowchart. Also, theory of weakly coupled resonators is applied to the gate structure to provide some formulas for simulating the outputs of networked weakly coupled resonators. Simulation results show that eight weakly coupled RF MEMS resonators can perform like a NAND gate with delay time less than 1 ns. Applying resonators with higher frequencies, would end up to less delay time. The simulation results show that most of the times the gate can produce output in less than 10 periods of oscillation. In four input cases, the gate needs more time to reach the output amplitude at desired level, while the correct phase is achieved in first few oscillations. As future work, amplifying some output signals to fasten output production may help to decrease the gate delay time to a few decades of ps.

6. Compliance with Ethical Standards

6.1. Conflict of interests:

M. Attar declares that he has no conflict of interest. R. Askari Moghadam declares that he has no conflict of interest.

6.2. Funding:

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6.3. Ethical approval:

This article does not contain any studies with human participants or animals performed by any of the authors.

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