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# Extracting Linear Relations from Gröbner Bases for Formal Verification of And-Inverter Graphs

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**Abstract.** Formal verification techniques based on computer algebra have proven highly effective for circuit verification. The circuit, given as an and-inverter graph, is encoded as a set of polynomials that automatically generates a Gröbner basis with respect to a lexicographic term ordering. Correctness of the circuit can be derived by computing the polynomial remainder of the specification. However, the main obstacle is the monomial blow-up during the rewriting of the specification, which leads to the development of dedicated heuristics to overcome this issue. In this paper, we investigate an orthogonal approach and focus the computational effort on rewriting the Gröbner basis itself. Our goal is to ensure the basis contains linear polynomials that can be effectively used to rewrite the linearized specification. We first prove the soundness and completeness of this technique and then demonstrate its practical application. Our implementation of this method shows promising results on benchmarks related to multiplier verification.

**Keywords:** Algebraic Reasoning, Gröbner Basis, Hardware Verification

## 1 Introduction

Formal verification techniques based on algebraic reasoning have emerged as highly effective tools for verifying hardware, particularly in the context of verifying arithmetic circuits on the gate-level. As digital systems become more complex, ensuring the correctness of such circuits is paramount, especially in safety-critical applications like cryptography and signal processing to prevent a repetition of infamous failures, such as the Pentium FDIV bug [28]. Established methods based on satisfiability solving (SAT) [4], or binary decision diagrams (BDDs) [7] often struggle with the complex non-linear structure of arithmetic circuits. In contrast, formal verification techniques based on theorem provers [29] or computer algebra, specifically those leveraging Gröbner bases, offer an effective alternative and have made significant progress in recent years [16, 18, 19, 26].

In the algebraic method, the circuit is given as an and-inverter graph (AIG) [20]. The graph is encoded as a set of polynomials, which are sorted according to a lexicographic term ordering, where for each gate in the circuit the output variable is always greater than the input variables of the gate. Hence, the leading

terms of the polynomial equations consist of single variables that are mutually disjoint. This property was called *unique monic leading term* (UMLT) in [16].

If such an ordering is chosen, the polynomials automatically form a Gröbner basis [5]. Informally said, a Gröbner basis is a mathematical construct that offers a decision procedure that guarantees soundness and completeness of the verification process. The correctness of the circuit is determined by computing the unique polynomial remainder of the specification polynomial, which represents the intended functionality of the circuit, modulo the Gröbner basis. The circuit fulfills the specification if and only if the final remainder is zero [17].

However, a major practical obstacle in using a lexicographic term ordering is the significant computational effort during the rewriting process, as the degree is not bounded. The size and degree of the intermediate reduction results typically increases tremendously, which is often deferred to as monomial blow-up [25]. Without specialized heuristics or preprocessing, the computation of the remainder often fails due to the rapid growth of the intermediate reduction results. To address this challenge, various preprocessing and rewriting algorithms have been developed, which syntactically or semantically analyze the input circuit to remove redundant information from the polynomial encoding, ultimately optimizing the reduction process and improving the efficiency of the verification.

*Related Work.* Advanced reduction engines designed for the automatic algebraic verification of multipliers given as AIGs are implemented in tools such as DYNPHASEORDEROPT [18], DYPOSUB [26], and AMULET2 [15, 16], including its variant TELUMA [14]. In [16] and the corresponding tool AMULET2 [15] the authors employ SAT solving to rewrite certain parts of the multiplier before applying an incremental column-wise verification algorithm. In a follow-up work [14] the usage of the external SAT solver could be removed by using a sophisticated algebraic encoding that also takes the polarity of literals into account. These techniques have been further enhanced by parallelization [23] and equivalence checking-based verification [21].

In [26] the authors present a dynamic rewriting approach in their tool DYPOSUB. After identifying and rewriting atomic blocks, they decide on the reduction order on the fly and backtrack if the size of intermediate reduction results exceeds a predetermined threshold. In upcoming work [18], the authors revisit and improve upon [26] by developing a dynamic rewriting approach that relies on an encoding that incorporates mixed signals. This encoding is more general than that presented in [14]. This approach has also been shown to successfully verify synthesized circuits.

While all of the discussed approaches employ various preprocessing and rewriting techniques, they share a common characteristic: they all rely on a lexicographic term ordering. *None of the related works have explored alternative term orderings, such as those that prioritize degree-based sorting to limit the degree during the reduction process.*

*Our contribution.* In this paper, we propose an alternative, orthogonal strategy that shifts the focus of the computational effort from rewriting the specification

polynomial to rewriting the Gröbner basis itself. The approach is based on the following observation:

If the specification polynomial is linear, a Gröbner basis with respect to a degree reverse lexicographic term ordering contains linear polynomials that suffice to derive correctness of the circuit.

Our first contribution is to derive the theoretical foundations of this technique, including a technical theorem that proves its soundness and completeness.

However, the computation of a single Gröbner basis for the whole circuit is practically infeasible due to the double-exponential complexity of computing a Gröbner basis and more importantly the *degree of the underlying ideal*. Our second contribution is a practical algorithm that splits the computation of the Gröbner basis into multiple smaller more manageable sub-problems. We evaluate our approach on a set of benchmarks for multiplier verification. The experimental results are promising and indicate that our approach offers a valuable addition to existing algebraic verification techniques.

The remainder of the paper is organized as follows. In Section 2 we introduce the necessary preliminaries. In Section 3 we show the theory of our approach and prove the soundness and completeness. We present a practical verification algorithm in Section 4, and discuss its implementation and the experimental evaluation in Section 5 before we conclude the paper in Section 6.

## 2 Preliminaries

In the first part of the preliminaries, Section 2.1, we introduce the theory of Gröbner bases following [5,6,8] and discuss key properties that are important for our approach. In the second part, Section 2.2, we present the necessary background on AIGs and how we can encode these graphs using polynomial equations.

### 2.1 Gröbner Basis

**Definition 1 (Term, Monomial, Polynomial, see [8, Chap. 2, Sec. 2, Def. 7]).** Let  $X = (x_1, \dots, x_n)$  be a set of variables and  $\mathbb{K}$  be a field. A monomial is a product of the form  $x_1^{e_1} \cdots x_n^{e_n}$ , with exponents  $e_1, \dots, e_n \in \mathbb{N}_0$ . The set of all monomials is represented by  $[X]$ . A term is a monomial multiplied by a constant, written as  $\alpha x_1^{e_1} \cdots x_n^{e_n}$  with  $\alpha \in \mathbb{K}$ . A polynomial  $p$  is a finite sum of such terms. We denote the number of terms in  $p$  by  $\text{size}(p)$ .

Throughout this section let  $\mathbb{K}[X] = \mathbb{K}[x_1, \dots, x_n]$  denote the ring of polynomials in variables  $x_1, \dots, x_n$  with coefficients in the field  $\mathbb{K}$ . We write polynomials in their canonical form. That is, monomials with equal monomials are merged by adding their coefficients; and terms with coefficients equal to zero are removed.

**Definition 2 (Degree).** The degree of a monomial  $\sigma = x_1^{e_1} \cdots x_n^{e_n}$  is the sum of its exponents, i.e.,  $\deg(\sigma) = |\sigma| = \sum_{i=1}^n e_i$ . The degree of a polynomial is the maximum degree of its terms.

The terms within a polynomial are sorted according to a total order to ensure a consistency for algebraic operations.

**Definition 3 (Total Order).** *A monomial order is a total order  $\prec$  such that for all distinct monomials  $\sigma_1, \sigma_2$  we have (i)  $\sigma_1 \prec \sigma_2$  or  $\sigma_2 \prec \sigma_1$ , (ii) every non-empty set of monomials has a smallest element and (iii)  $\sigma_1 \prec \sigma_2 \Rightarrow \tau\sigma_1 \prec \tau\sigma_2$  for any term  $\tau$ .*

**Definition 4 (Lexicographic Order, see [8, Chap. 2, Sec. 2, Def. 3]).** *Let  $\sigma_1 = x_1^{u_1} \cdots x_n^{u_n}$  and  $\sigma_2 = x_1^{v_1} \cdots x_n^{v_n}$  be two monomials. We say that  $\sigma_1 \prec_{\text{lex}} \sigma_2$ , if there exists an index  $i$  such that with  $u_j = v_j$  for all  $1 \leq j < i$ , and  $u_i < v_i$ .*

**Definition 5 (Degree Reverse Lexicographic Order, see [8, Chap. 2, Sec. 2, Def. 6]).** *Let  $\sigma_1 = x_1^{u_1} \cdots x_n^{u_n}$  and  $\sigma_2 = x_1^{v_1} \cdots x_n^{v_n}$  be two monomials. We say that  $\sigma_1 \prec_{\text{drl}} \sigma_2$ , if  $|\sigma_1| < |\sigma_2|$  or if  $|\sigma_1| = |\sigma_2|$  and there exists an index  $i$  such that  $u_j = v_j$  for all  $i < j \leq n$ , and  $u_i > v_i$ .*

Since every polynomial  $p \in \mathbb{K}[X]$  contains only a finite number of monomials, and these terms are sorted according to a fixed total order, we can identify the largest monomial in  $p$ . This is referred to as the *leading monomial* of  $p$  and denoted as  $\text{lm}(p)$ . If  $p = c\tau + \cdots$  and  $\text{lm}(p) = \tau$ , then  $\text{lc}(p) = c$  is called the *leading coefficient* and  $\text{lt}(p) = \text{lc}(p)\text{lm}(p) = c\tau$  is called the *leading term* of  $p$ . The *tail* of  $p$  is defined by  $\text{tail}(p) = p - \text{lt}(p)$ .

**Definition 6 (Ideal).** *A nonempty subset  $I \subseteq \mathbb{K}[X]$  is called an ideal if*

$$\forall u, v \in I : u + v \in I \quad \text{and} \quad \forall w \in \mathbb{K}[X] \forall u \in I : wu \in I.$$

*If  $I \subseteq \mathbb{K}[X]$  is an ideal, then a set  $G = \{g_1, \dots, g_m\} \subseteq \mathbb{K}[X]$  is called a basis of  $I$  if  $I = \{h_1g_1 + \cdots + h_mg_m \mid h_1, \dots, h_m \in \mathbb{K}[X]\}$ , i.e., if  $I$  consists of all the linear combinations of  $g_i$  with polynomial coefficients. We denote this by  $I = \langle G \rangle$  and say  $I$  is generated by  $G$ .*

An ideal  $I = \langle G \rangle \subseteq \mathbb{K}[X]$  can be interpreted as an equational theory, where the basis  $G = \{g_1, \dots, g_m\}$  serves as the set of axioms. The ideal  $I = \langle G \rangle$  consists of precisely those polynomials  $f$  for which the equation  $f = 0$  can be derived from the axioms  $g_1 = \cdots = g_m = 0$  through repeated application of the rules  $u = 0 \wedge v = 0 \Rightarrow u + v = 0$  and  $u = 0 \Rightarrow wu = 0$ .

To check whether a polynomial  $f \in \mathbb{K}[X]$  is contained in an ideal  $I$ , we want to solve the so-called *ideal membership problem*: Given a polynomial  $f \in \mathbb{K}[X]$  and an ideal  $I = \langle G \rangle \subseteq \mathbb{K}[X]$ , determine if  $f \in I$ .

**Definition 7 (Remainder).** *The process of finding a remainder with respect to a set of polynomials  $G$  is equal to computing the remainder of a polynomial division, but extended to multiple divisors, until no further division is possible. The result is a polynomial that represents the equivalent class modulo the ideal generated by  $G$ . We write  $p \rightarrow_G g$  to denote that  $g$  is the polynomial remainder of  $p$  modulo  $G$  and we also say “ $p$  is reduced by  $G$ ”.*

In general, an ideal  $I$  has many bases that generate  $I$ . We are particularly interested in bases with certain structural properties that allow to uniquely answer the ideal membership problem. Such bases are called *Gröbner bases* [5].

**Lemma 1** (see [8, Chap. 2, Sec. 5, Cor. 6]). *Every ideal  $I \subseteq \mathbb{K}[X]$  has a Gröbner basis w.r.t. a fixed total order.*

Given an arbitrary basis of an ideal, a Gröbner basis can be computed using Buchberger’s algorithm that repeatedly computes so-called S-Polynomials. These S-Polynomials are reduced by the polynomials that are already in the current basis, i.e., calculating the remainder of polynomial division, and non-zero remainders are added to the ideal basis. These steps are repeated until the basis is saturated. If all S-Polynomials reduce to zero the set of ideal generators is a Gröbner basis [5]. While it is known that Buchberger-like algorithms for computing Gröbner bases, such as Buchberger’s seminal algorithm [5] or Faugère’s  $F_4$  [9] algorithm, have a worst-case time complexity double exponential in the number of variables. Still, in practice, these algorithms behave in general way better for  $\prec_{\text{drl}}$  than for other monomial orders, such as  $\prec_{\text{lex}}$ .

We will not introduce this process more formally, as we will treat the computation of a Gröbner basis as a black-box technique in our approach. The following properties are more important for us.

**Lemma 2** (see [8, Chap. 2, Sec. 6, Prop. 1]). *If  $G = \{g_1, \dots, g_m\}$  is a Gröbner basis, then every  $f \in \mathbb{K}[X]$  has a unique polynomial remainder  $r$  with respect to  $G$ . Furthermore it holds that  $f - r \in \langle G \rangle$ , which implies that  $f$  is contained in the ideal  $I = \langle G \rangle$  if, and only if,  $f \rightarrow_G 0$ .*

Depending on the information one seeks, some Gröbner bases are more useful than others. Gröbner bases w.r.t.  $\prec_{\text{lex}}$  are the tool of choice for solving polynomial systems but are, in general, more expensive to compute than degree-based Gröbner bases. Yet, *change of order* algorithms, such as the seminal FGLM one [11] can convert a Gröbner basis into another one for different order. In our setting of verifying AIG the complexity would be in  $O(n2^{3n})$ , where  $n$  is the number of input variables of the AIG. Hence, for large  $n$ , this is impractical. Variants of FGLM exploiting the structure of the input and output Gröbner bases under some genericity assumptions exist, we can mention [2, 10, 12, 27], but they are mostly designed for solving polynomial systems. As a consequence, they consider the input Gröbner basis to be for a degree-based order, such as  $\prec_{\text{drl}}$ , and the output Gröbner basis to be for  $\prec_{\text{lex}}$ .

## 2.2 And-Inverter Graphs

An *and-inverter graph* (AIG) [20] is a special case of a directed acyclic graph (DAG). They are useful tools to represent Boolean functions and logic circuits and provide a compact and efficient way to describe logical expressions.

**Definition 8 (AIG).** *An AIG operates over Boolean variables. Every node expresses a logical conjunction between its two input variables, which are depicted by incoming edges in the lower part of the node. We distinguish two types of inputs, primary inputs (of the graph) and intermediate nodes. Outputs of the node are represented by an edge in the upper half. If an edge is marked, it indicates that the variable is negated.*

**Definition 9 (Specification).** *The specification of an AIG is a polynomial equation  $\mathcal{S} \in \mathbb{K}[X]$  that relates the outputs of an AIG to its primary inputs.*

Together with the specification polynomial, we fix the polynomial ring  $\mathbb{K}[X]$  of the encoding. Although, the nodes in an AIG compute logical conjunction over Boolean variables, the specification can encode richer relations. Hence, the encoding is not restricted to the Boolean ring  $\mathbb{B}[X]$ , but may include different coefficient domains, such as integers or rationals.

**Definition 10 (Gate Polynomials).** *Each node in an AIG can be encoded by a corresponding polynomial equation that models the logical conjunction. Nodes in an AIG, raise four types of equations, depending if either none, the first, the second, or both inputs are negated. Let  $g$  be an AIG node with inputs  $a, b$ :*

<i>Gate constraint</i>	$\Rightarrow$	<i>Gate polynomial</i>
$g = a \wedge b$	$\Rightarrow$	$g - ab = 0$
$g = \neg a \wedge b$	$\Rightarrow$	$g - (1 - a)b = g + ab - b = 0$
$g = a \wedge \neg b$	$\Rightarrow$	$g - a(1 - b) = g + ab - a = 0$
$g = \neg a \wedge \neg b$	$\Rightarrow$	$g - (1 - a)(1 - b) = g - ab + b + a - 1 = 0$

The correctness of the encoding can easily be checked by truth tables. Furthermore, observe that the degree of the gate polynomials is always two.

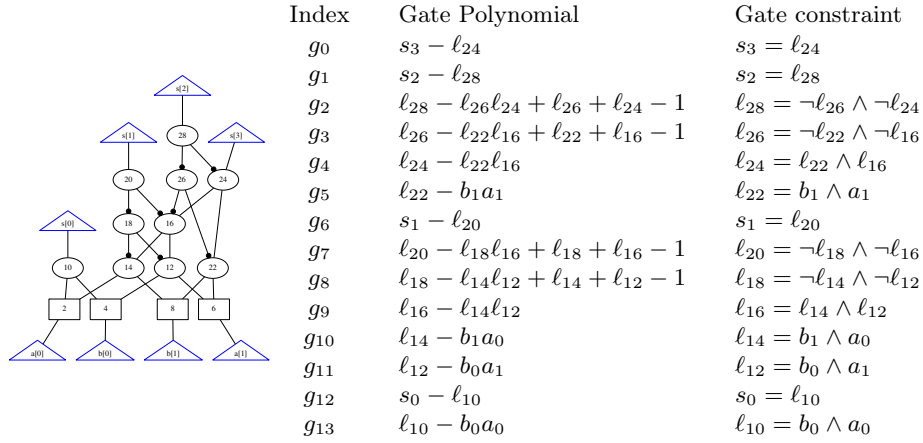
**Definition 11 (Boolean Input Polynomial).** *For every primary input  $a_i$  of the AIG we define a corresponding Boolean input polynomial  $a_i(a_i - 1) = a_i^2 - a_i = 0$  that encodes that the variable can only take the values 0 and 1.*

As we will only consider polynomial equations with right hand side zero, we will from now on shorten our notation and write “ $f$ ” instead of “ $f = 0$ ”.

*Example 1.* Figure 1 shows an AIG representing a 2-bit multiplier. We denote the primary inputs by  $a_0, a_1, b_0, b_1$  and outputs by  $s_0, s_1, s_2, s_3$ . The internal nodes are denoted by  $\ell_i$ . The right hand side of Figure 1 lists the gate constraints as well as the corresponding gate polynomials. We furthermore list the Boolean input polynomials and the specification polynomial  $\mathcal{S} \in \mathbb{Q}[X]$ , which relates that  $S = A \cdot B$ , for  $S = \sum_{i=0}^3 2^i s_i$ ,  $A = \sum_{i=0}^1 2^i a_i$ , and  $B = \sum_{i=0}^1 2^i b_i$ .

### 3 Verification using Degree Reverse Lexicographic Order

In this section we will lay out the theoretical foundation of our proposed approach for extracting linear relations from the Gröbner basis that is used for reduction.



Boolean Input Polynomials:  $a_1^2 - a_1, a_0^2 - a_0, b_1^2 - b_1, b_0^2 - b_0$   
 Specification  $\mathcal{S}$ :  $8s_3 + 4s_2 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$

**Fig. 1.** AIG and polynomial encoding of a 2-bit multiplier in the ring  $\mathbb{Q}[X]$ .

Existing algebraic verification techniques for acyclic graphs encode the circuit as a polynomial using a lexicographic term ordering where the variables are sorted according to a reverse topological term ordering (RTTO) [24]. This has the benefit that due to repeated application of Buchberger's product criterion, see [8, Chap. 2, Sec. 10, Prop. 1], the set of gate polynomials together with the Boolean input polynomials automatically form a Gröbner basis [17]. Since the leading terms of the gate polynomials consist of one single variable, polynomial division comes down to substitution. The variables in the specification are substituted by the corresponding tails of the gate polynomials until no further rewriting is possible. The graph fulfills its specification if, and only if, the final result is zero. If the result is non-zero, the remainder polynomial consists of primary inputs only and can be used to derive a counter example.

Generally, this implies that the degree of the intermediate reduction results increases, since the tails of the gate polynomials have a higher degree than their linear leading terms. Substituting those variables in non-linear monomials has the potential to lead to a monomial blow-up during the reduction. A study in [25] showed that the intermediate reduction results for 16-bit multipliers can have more than  $10^6$  monomials.

*Example 2.* Consider again the polynomials of Example 1. Initially  $\text{size}(\mathcal{S}) = 8$  and  $\text{deg}(\mathcal{S}) = 2$ . After four rewriting steps we have the following intermediate reduction result:  $\mathcal{S} \rightarrow_{\{g_1, g_2, g_3, g_4\}} 4l_{24}l_{22}l_{16} - 4l_{24}l_{22} - 4l_{24}l_{16} + 8l_{24} - 4l_{22}l_{16} + 4l_{22} + 2s_1 + 4l_{16} + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$  which has degree 3 and consists of 13 monomials.

In this paper, we will now apply an orthogonal approach. We impose a different ordering on the set of gate polynomials that takes the degree of the poly-



nomials into account. That is, we compute a Gröbner basis based on the degree reverse lexicographic monomial ordering, where the monomials in a polynomial are first sorted according to their degree.

Our approach is based on the following result that we prove in Theorem 1: *If the specification polynomial is linear, then the ideal membership of the specification can be decided using only the linear polynomials of the Gröbner basis.*

We linearize the specification by replacing all non-linear monomials  $\sigma_i$  in  $\mathcal{S}$  with new extension variables  $t_i$ . For each replacement we generate a new polynomial constraint  $t_i - \sigma_i$  and add it to the set of gate polynomials. This idea is not novel and was, for instance, used in [22], where the variables  $t_i$  are called tableau variables. The following lemma proves that if the non-linear specification  $\mathcal{S}$  is contained in the ideal generated by the gate polynomials, then the linearized specification  $\mathcal{S}_{\text{lin}}$  is contained in the ideal generated by the gate polynomials and *extension polynomials*.

**Lemma 3.** *Let  $p \in \mathbb{K}[X]$ ,  $I \subseteq \mathbb{K}[X]$ . Let  $\Sigma = \{t_i - \sigma_i \mid t_i \notin X \wedge \sigma_i \in p \wedge \deg(\sigma_i) > 1\}$ . Let  $p_{\text{lin}}$  be the polynomial where every non-linear monomial of  $p$  is replaced by a corresponding extension variable  $t_i$ . Then we have  $p \in I$  if and only if  $p_{\text{lin}} \in I + \langle \Sigma \rangle$ .*

*Proof.* Let  $p = \sum_{\sigma_i \in p} c_i \sigma_i$ , where the  $c_i$ 's are in  $\mathbb{K}$ . By definition, we can write  $p_{\text{lin}} = \sum_{\sigma_i \in p} c_i t_i$ . Thus,  $p_{\text{lin}} = \sum_{\sigma_i \in p} c_i (t_i - \sigma_i) + \sum_{\sigma_i \in p} c_i \sigma_i$ . By hypothesis, the first sum is in  $\langle \Sigma \rangle$  and the second one, which is  $p$ , only depends in variables  $X$ . Therefore, if  $p \in I$ , then  $p_{\text{lin}} \in I + \langle \Sigma \rangle$ . Conversely, if  $p_{\text{lin}} \in I + \langle \Sigma \rangle$ , then  $p \in (I + \langle \Sigma \rangle) \cap \mathbb{K}[X] = I$  by construction of  $I + \langle \Sigma \rangle$ .

The following theorem proves soundness and completeness of our observation. That is, if we want to show ideal membership of a linear polynomial, the Gröbner basis of the ideal contains a set of linear polynomials  $G_1$  that suffice for the deriving the ideal membership, all non-linear polynomials of the Gröbner basis can be neglected. This will shift the computational difficulties from the reduction to the Gröbner basis generation.

**Theorem 1.** *Let  $p \in \mathbb{K}[X]$  with  $\deg(p) = 1$ ,  $I \subseteq \mathbb{K}[X]$  be an ideal. Let  $G$  be a Gröbner basis of  $I$  with respect to  $\prec_{\text{drl}}$  and let  $G_1 = \{g \in G \mid \deg(g) \leq 1\}$ . We have  $p \in I$  if and only if  $p \rightarrow_{G_1} 0$ . In particular,  $p = \alpha_1 g_1 + \dots + \alpha_m g_m$  with  $g_i \in G_1$ ,  $\alpha_i \in \mathbb{K}$ .*

*Proof.* First, let us observe that if  $G_1$  contains a non-zero constant polynomial, then  $I = \mathbb{K}[X]$  and  $p$  necessarily reduces to 0 by  $G_1$ .

We now assume that  $G_1$  only contains polynomials of degree 1. For  $g \in G_1$ , we write  $g = \text{lt}(g) + \text{tail}(g)$ , with  $\deg(\text{lm}(g)) = 1$  and  $\deg(\text{tail}(g)) \leq 1$ . Since  $\deg(\text{lm}(p)) = 1$  the division algorithm for computing the reduction of  $p$  by  $G$ , see [8, Chap. 2, Sec. 3], will only select polynomials in  $G$  whose leading monomials also have degree 1, i.e. those in  $G_1$ . The reduction step will replace  $p$  by  $p - cg = \text{tail}(p) - c \text{tail}(g)$ , for  $c \in \mathbb{K}$ , which has degree less or equal to 1.

Since  $p \in I$  if, and only if,  $p \rightarrow_G 0$ , we have  $p \in I$  if, and only if,  $p \rightarrow_{G_1} 0$ .

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**Algorithm 1:** Linear Gröbner basis reduction
 

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**Input** : Circuit  $C$  in AIG format, Specification polynomial  $\mathcal{S}$   
**Output:** Determine whether  $C$  fulfills the specification  
 1  $G_{\text{init}} \leftarrow \text{Gate-Polynomials}(C) \cup \text{Boolean-Input-Polynomials}(C)$ ;  
 2  $\mathcal{S}_{\text{lin}}, G_{\text{ext}} \leftarrow \text{Linearize}(\mathcal{S})$ ;  
 3  $G_{\text{drl}} \leftarrow \text{Compute-}\prec_{\text{drl}}\text{-Gröbner-Basis}(G_{\text{init}} \cup G_{\text{ext}})$ ;  
 4  $G_1 \leftarrow \{g \mid g \in G_{\text{drl}} \wedge \deg(g) \leq 1\}$ ;  
 5 **while**  $\text{lm}(\mathcal{S}_{\text{lin}}) \in \{\text{lm}(g) \mid g \in G_1\}$  **do**  
 6      $p_{\text{lin}} \leftarrow g \in G_1$  such that  $\text{lm}(g) = \text{lm}(\mathcal{S}_{\text{lin}})$ ;  
 7     **if**  $\nexists p_{\text{lin}}$  **then return**  $\perp$ ;  
 8      $\mathcal{S}_{\text{lin}} \leftarrow \text{Linear-Reduce}(\mathcal{S}_{\text{lin}}, p_{\text{lin}})$ ;  
 9 **end**  
 10 **return**  $\mathcal{S}_{\text{lin}} = 0$

---

We focus our discussion on the use case of formally verifying an AIG. *However, it is important to emphasize that the theory, and in particular the result of Theorem 1, is not restricted to AIGs and can be applied to general DAGs.* The key property of the graph for deriving a total degree reverse lexicographic order is that it must be *acyclic*.

The conclusion of Theorem 1 moreover shows that we can significantly simplify the algorithm for checking the ideal membership of  $\mathcal{S}$ . Instead of repeated polynomial substitution, with potential non-linear intermediate reduction results, we pick  $g_i \in G_1$ , such that  $\text{lm}(g_i) = \text{lm}(\mathcal{S})$ , multiply  $g_i$  by a constant  $\alpha_i$  such that  $\text{lc}(\mathcal{S}) = -\alpha_i \text{lc}(g_i)$  and add those two polynomials. Hence, we have replaced polynomial division by linear polynomial operations.

Therefore, we can apply the following approach to verify that an AIG fulfills its specification, see Alg. 1. We first encode the graph as a set of polynomials  $G_{\text{init}}$  (line 1), and linearize the specification (line 2) as described in Lemma 3. The set  $G_{\text{ext}}$  contains the extension polynomials. In the next step we compute a Gröbner basis w.r.t.  $\prec_{\text{drl}}$  (line 3) and extract the linear polynomials  $G_1$  (line 4). We calculate the remainder of the specification modulo the linear elements of the Gröbner basis (lines 5-8) until no further reduction is possible and return whether the final result is zero. The correctness of Alg. 1 follows from Theorem 1.

*Example 3.* Consider again the AIG of Example 1. First of all we define four extension variables  $t_{ij}$  to encode the non-linear terms  $a_i b_j$  for  $i, j \in \{0, 1\}$  and rewrite the specification to  $8s_3 + 4s_2 + 2s_1 + s_0 - 4t_{11} - 2t_{10} - 2t_{01} - t_{00}$ . The four polynomial equations  $t_{ij} - a_i b_j$  are added to the set of gate polynomials and we compute a Gröbner basis w.r.t.  $\prec_{\text{drl}}$ . The full Gröbner basis consisting of 52 polynomials is listed in Appendix A.

Important for us are the first thirteen elements of the Gröbner basis, as those are the linear polynomials  $G_1$ :

$$\begin{aligned}
g_1 &= \ell_{10} - t_{00} & g_8 &= \ell_{22} - t_{11} \\
g_2 &= s_0 - \ell_{10} & g_9 &= \ell_{24} - \ell_{16} \\
g_3 &= \ell_{12} - t_{10} & g_{10} &= \ell_{26} - \ell_{24} + \ell_{16} + t_{11} - 1 \\
g_4 &= \ell_{14} - t_{01} & g_{11} &= \ell_{28} + 2\ell_{24} - \ell_{16} - t_{11} \\
g_5 &= \ell_{18} - \ell_{16} + t_{01} + t_{10} - 1 & g_{12} &= s_2 - \ell_{28} \\
g_6 &= \ell_{20} + 2\ell_{16} - t_{01} - t_{10} & g_{13} &= s_3 - \ell_{24} \\
g_7 &= s_1 - \ell_{20}
\end{aligned}$$

We derive that  $\mathcal{S} \in \langle G_1 \rangle$  as  $\mathcal{S} = 8g_{13} + 4g_{12} + 4g_{11} + 2g_7 + 2g_6 + g_2 + g_1$ .

In practice, however line 3 of Alg. 1 turns out to be a bottleneck, computing a single  $\prec_{\text{drl}}$ -Gröbner basis does not scale for larger AIGs. We have also seen in Example 1 that 39 out of 52 polynomials in the computed Gröbner basis are non-linear. While these polynomials are needed to compute the full Gröbner basis of the ideal, they are not required for solving the ideal membership problem of the linear specification. Furthermore, from the 13 linear polynomials, only 7 are used to generate the specification. Hence, our generated Gröbner basis contains redundant and/or useless information. We will discuss a method to reduce the overhead by computing local Gröbner bases in the following section.

## 4 Locally extracting Linear Polynomials

The core idea of the optimized approach is to start from a  $\prec_{\text{lex}}$ -Gröbner basis and incrementally extract linear polynomials from a smaller set of gate polynomials instead of computing a single full  $\prec_{\text{drl}}$ -Gröbner basis for the whole input AIG. The algorithm is outlined in Alg. 2 and will be explained in more detail throughout the remainder of this section.

In a nutshell, we first encode the circuit using a lexicographic term ordering (line 1) and linearize the specification polynomial (line 2) with respect to the given circuit. After some preprocessing where we extract easily derivable linear polynomials (line 3), we rewrite the specification by generating linear polynomials on the fly (lines 4–9). We pick the gate polynomial  $p$  that has the same leading term as the intermediate reduction result (line 5) and compute a  $\prec_{\text{drl}}$ -Gröbner basis for a sub-circuit of  $C$  that includes  $p$  (line 6) to receive the linearized polynomial  $p_{\text{lin}}$  that we use for reducing the specification (line 7). Let us now go into more detail of every step.

*Encoding.* The AIG is encoded using gate polynomials and Boolean input polynomials as described in Def. 10 and 11 using a lexicographic term ordering. We choose a row-wise variable ordering that sorts variables based on their distance to the inputs. If nodes have an equal distance, we sort according to the value of the AIG node. For example, we would sort the variables in Example 1 as  $a_0 \prec_{\text{lex}} b_0 \prec_{\text{lex}} a_1 \prec_{\text{lex}} b_1 \prec_{\text{lex}} \ell_{10} \prec_{\text{lex}} \ell_{12} \prec_{\text{lex}} \ell_{14} \prec_{\text{lex}} \ell_{22} \prec_{\text{lex}} s_0 \prec_{\text{lex}} \ell_{16} \prec_{\text{lex}} \ell_{18} \prec_{\text{lex}} \ell_{20} \prec_{\text{lex}} \ell_{24} \prec_{\text{lex}} \ell_{26} \prec_{\text{lex}} \ell_{28} \prec_{\text{lex}} s_1 \prec_{\text{lex}} s_3 \prec_{\text{lex}} s_2$ . In this order the output variable of a gate is always greater than its input variables, which automatically generates a  $\prec_{\text{lex}}$ -Gröbner basis.

---

**Algorithm 2:** Verification-via-Locally-extracting-Linear-Polynomials
 

---

**Input** : Circuit  $C$  in AIG format, Specification polynomial  $\mathcal{S}$   
**Output:** Determine whether  $C$  fulfills the specification  
 1  $G_{\text{init}} \leftarrow \text{Row-Wise-RTTO-Polynomial-Encoding}(C)$ ;  
 2  $\mathcal{S}_{\text{lin}}, G_{\text{ext}} \leftarrow \text{Linearize-Spec-wrt-AIG}(\mathcal{S}, G_{\text{init}})$ ;  
 3  $G \leftarrow \text{Preprocessing}(G_{\text{ext}})$  ▷See Section 4.1  
 4 **while**  $\text{lm}(\mathcal{S}_{\text{lin}}) \in \{\text{lm}(g) | g \in G\}$  **do**  
 5      $p \leftarrow g \in G$  such that  $\text{lm}(g) = \text{lm}(\mathcal{S}_{\text{lin}})$ ;  
 6      $p_{\text{lin}} \leftarrow \text{Linearize-Single-Polynomial}(p, G)$  ▷See Section 4.2  
 7     **if**  $p_{\text{lin}} = 0$  **then return**  $\perp$ ;  
 8      $\mathcal{S}_{\text{lin}} \leftarrow \text{Linear-Reduce}(\mathcal{S}_{\text{lin}}, p_{\text{lin}})$ ;  
 9 **end**  
 10 **return**  $\mathcal{S}_{\text{lin}} = 0$

---

Theorem 4 in [17] has shown that we can locally rewrite elements of the  $\prec_{\text{lex}}$ -Gröbner basis without jeopardizing the Gröbner basis property as long as the leading monomials remain the same. We apply the same technique and locally rewrite gate polynomials from quadratic to linear polynomials that will be used in the reduction.

*Linearization of the Specification.* Lemma 3 provides us with a methodology on how to linearize the specification  $\mathcal{S}$  by introducing extension variables to represent non-linear terms. However, some of the terms might already be contained in the polynomial encoding of the circuit. For those terms we can simply use the corresponding leading term in the specification. We first swipe through the set of gate polynomials and check whether the non-linear tail of a gate polynomial is contained in the specification. If this is the case, we replace the non-linear term by the corresponding leading term.

For instance, in Example 3 we have the gate polynomial  $\ell_{22} - a_1 b_1$ . Hence, we do not require the extension variable  $t_{11}$  to linearize  $\mathcal{S}$ . This equality  $\ell_{22} = t_{11}$  is also contained as polynomial  $g_8$  in the computed  $\prec_{\text{drl}}$ -Gröbner basis.

All non-linear terms of  $\mathcal{S}$  that cannot be linearized using gate polynomials we introduce extension variables as described in Section 3.

At this point, our encoding consists of a linear specification polynomial and a set of quadratic gate polynomials and Boolean input polynomials that generate a Gröbner basis w.r.t. a lexicographic term ordering. The following subsections present how we linearize elements of the Gröbner basis.

#### 4.1 Preprocessing

The goal of preprocessing is to eliminate variables and derive linear polynomials in the  $\prec_{\text{lex}}$ -Gröbner basis that can be identified using simple heuristics. We employ three steps of rewriting, depicted in Alg. 3.

**Algorithm 3:** Preprocessing

---

**Input** : Set of polynomial encodings of gate constraints  $G$   
**Output**: Rewritten Set of Polynomial encodings  $G$

- 1  $G \leftarrow \text{Merge-Nodes-with-Equal-Inputs}(G)$ ;
- 2  $G \leftarrow \text{Eliminate-Positive-Nodes}(G)$ ;
- 3  $G \leftarrow \text{Propagating-Equivalent-Nodes}(G)$ ;
- 4 **return**  $G$ ;

---

*Merge Nodes with Equal Inputs.* If multiple AIG nodes  $\ell_i, \ell_j$  have the same inputs  $a, b$ , we can express one gate polynomial using the other. For instance, in our running Example 1 the nodes  $\ell_{24} = \ell_{22}\ell_{16}$  and  $\ell_{26} = (1 - \ell_{22})(1 - \ell_{16})$  would be such a set of AIG nodes.

Every gate polynomial of an AIG node has degree two, and the quadratic term is the product of the input nodes. Hence, the non-linear term in those gate polynomials that have the same inputs is the same. We remove the non-linear term of the topologically larger polynomial by adding or subtracting the smaller polynomial. For instance, we derive  $\ell_{26} - \ell_{24} + \ell_{22} + \ell_{16} - 1$ .

Furthermore, if at least one input  $a, b$  has a different polarity in  $\ell_i$  and  $\ell_j$ , we immediately can derive that the product  $\ell_i\ell_j$  is equal to zero. Let  $\ell_i - \bar{a}\bar{b}$ ,  $\ell_j - \hat{a}\hat{b}$  be the corresponding gate polynomials, where  $\bar{a}$  and  $\hat{a}$  represent the polarity of  $a$ . We have  $\ell_i\ell_j - \bar{a}\bar{a}\hat{a}\hat{b} = 0$ , since  $(\bar{a} = 1 - \hat{a}) \vee (\bar{b} = 1 - \hat{b})$  holds. Thus, we can always remove the term  $\ell_i\ell_j$  in a possible parent node, for instance the monomial  $\ell_{26}\ell_{24}$  in  $\ell_{28}$  in Example 1 can be removed.

*Eliminate Positive Nodes.* In this step we eliminate nodes which are only non-negated inputs to other nodes in the graph. This heuristic was already considered in [14]. Since we restrict this heuristic to positive inputs, we can simply replace every occurrence of the node by the corresponding tail in the gate polynomial of the parent node. This, will increase the degree of the parent polynomial. However, we can check whether parts of the new tail term of the parent are equal to the tail term of another gate polynomial. If yes, we can reduce the tail term and include the leading term. This will decrease the temporal increase of the polynomial degree and furthermore will impose a node sharing which will be useful in later Gröbner basis computations. For instance, consider the polynomials  $f - da, e - ca, d - cb$ . We can derive  $f - cba = f - eb$ .

*Propagating Equivalent Nodes.* If at any point in the rewriting we derive a linear polynomial of the form  $\ell_i - \ell_j$  or  $\ell_i + \ell_j - 1$  we know that  $\ell_i$  is equal to either  $\ell_j$  or to its negation  $1 - \ell_j$ . We propagate this information by eliminating the topologically larger node  $\ell_i$  from the polynomial encoding. We choose to eliminate  $\ell_i$  and not  $\ell_j$  in order to not mess up the reverse topological term ordering for parent nodes of  $\ell_j$ . Propagation of equivalent nodes may not directly lead to linear gate polynomials, but helps to reduce the overall number of variables.

---

**Algorithm 4: Linearize-Single-Polynomial**


---

**Input** : Polynomial  $p$ , Polynomial system  $G$   
**Output**: Linear polynomial  $p_{\text{lin}}$  or 0

```

1  $v \leftarrow \text{lm}(p); d \leftarrow 3;$ 
2 while  $d \leq \text{dist}(v)$  do
3    $C_v \leftarrow \{v\} \cup \{\text{Children-up-to-Distance}(v, d)\} \cup \{\text{Siblings}(v)\};$ 
4    $C_v \leftarrow C_v \cup \{\text{Parents}(C_v)\};$ 
5    $G_v \leftarrow \text{Gate-Polynomials}(C_v, G) \cup \text{Boolean-Input-Polynomials}(C_v);$ 
6    $G_{\text{drl}} \leftarrow \text{Compute-}\prec_{\text{drl}}\text{-Gröbner-Basis}(G_v);$ 
7   if  $\exists p_{\text{lin}} \in G_{\text{drl}}$  such that  $\text{deg}(p_{\text{lin}}) = 1 \wedge \text{lm}(p_{\text{lin}}) = v$  then return  $p_{\text{lin}};$ 
8    $d \leftarrow d + 1;$ 
9 end
10 return 0;
    
```

---

## 4.2 Linear Reduction

After preprocessing we repeatedly rewrite the linearized specification by the polynomial  $p$  in the Gröbner basis that has the same leading monomial as the specification (line 5 in Alg. 2). For doing so, we need to linearize  $p$ . The pseudo-code is listed in Alg. 4. By Theorem 1, we know that a  $\prec_{\text{drl}}$ -Gröbner basis of a circuit must contain a linear polynomial  $p_{\text{lin}}$  with the same leading monomial as  $p$ . If this condition is not met, then the circuit does not satisfy the specification, as we cannot further reduce  $\mathcal{S}$ .

Let  $v = \text{lm}(p)$ . We aim to compute a Gröbner basis w.r.t. a  $\prec_{\text{drl}}$ -ordering for a sub-circuit  $C_v$  of  $C$ . The sub-circuit  $C_v$  is constructed by including  $v$  and all children nodes of  $v$  up to a maximum distance  $d$ . Initially, we set  $d = 2$ . If, during this process, we encounter a child node that already has a linear polynomial representation, we do not further add its children. This allows us to avoid unnecessary computations by excluding parts of the circuit that have already been simplified. Additionally, we include all smaller sibling nodes of  $v$ . Siblings are nodes that share at least one child with  $v$ . Moreover, we collect all parent nodes whose children are already included in the current set of nodes. This ensures that all relevant dependencies in the sub-circuit are captured.

This set of nodes represents the part of the circuit on which we will compute a local  $\prec_{\text{drl}}$ -Gröbner basis. The goal is to make the Gröbner basis just big enough such that it contains a linear polynomial with leading term  $v$ .

If this local Gröbner basis does not contain the expected linear polynomial, it suggests that the sub-circuit  $C_v$  is insufficient to capture the desired behavior. In such cases, we repeat the process with an increased distance  $d$  of the sub-circuit by adding more nodes. This iterative process continues until either a linear polynomial is found, or, in the worst case we have computed a full  $\prec_{\text{drl}}$ -Gröbner basis for all gate polynomials that are topologically smaller than  $v$ .

While this approach guarantees the completeness of the verification process, it comes with a practical limitation: computational complexity. If the sub-circuit

grows too large (i.e., if too many nodes need to be added to  $C_v$ ), the computation of the  $\prec_{\text{drl}}$ -Gröbner basis becomes infeasible in practice.

## 5 Experimental Evaluation

We evaluate our proposed approach on a set of multiplier benchmarks for different input bit-widths  $n$ . For all the circuits we have  $\mathcal{S} = \sum_{i=0}^{2n} 2^i s_i - (\sum_{i=0}^n 2^i a_i) \cdot (\sum_{i=0}^n 2^i b_i)$ , hence choose  $\mathbb{K} = \mathbb{Q}$ . Since all the leading coefficients of the gate polynomials are 1, the computation will actually stay in the ring  $\mathbb{Z}[X] \subseteq \mathbb{Q}[X]$  [16].

### 5.1 Implementation

We implement Alg. 2 in our tool MULTILING, written in C++. We employ the following features:

- MULTILING uses the polynomial arithmetic module from AMULET2 [15], which is targeted towards polynomial arithmetic where the variables represent Boolean values and the coefficients are integer values. In particular, the arithmetic engine automatically includes reasoning over the Boolean input polynomials, by reducing exponents, i.e., it calculates  $x \cdot x = x$  internally.
- We sort the variables based on their minimum distance to the primary inputs to sort all extension variables next to the primary inputs, which gave us better practical results than the column-wise variable order from AMULET2.
- As a consequence of the row-wise order, we do not apply an incremental column-wise reduction algorithm [17], but rewrite the complete specification.
- For computing the  $\prec_{\text{drl}}$ -Gröbner basis, we use the MSOLVE [3] library. Since MSOLVE is designed for general purposes, we have to explicitly provide the Boolean input polynomials.
- If the linearization of individual polynomials fails and the distance of the node to the primary inputs is below six, we switch to non-linear rewriting as a fall-back option.
- In contrast to AMULET2, we do not support proof logging at the moment, as have not yet annotated MSOLVE with corresponding proof logging steps. This is part of future work.

In case of acceptance, we will prepare an artifact that will be submitted to the voluntary artifact evaluation of TACAS.

### 5.2 Setup

We run our experiments on a Intel i7-1260P CPU. The time is listed in rounded seconds (wall-clock time). The time limit for the aoki-benchmarks is 300 s, for the ABC-benchmarks it is set to 1200 s. We set the memory limit to 1000 MB. We compare MULTILING against the algebraic approaches of AMULET2 [15], TELUMA [14], and DYNPHASEORDEROPT [18]. The tools of related works [23] and [21] are not publicly available.

ABC-benchmarks			Related work			MULTILING			
$n$	Synthesis	Nodes	[14]	[15]	[18]	Time	MergedNodes	PosNodes	LocalGB
32	resyn	7840	0.1	TO	0.2	0.3	1948	1	10
32	resyn2	7840	0.1	TO	0.3	0.3	1948	1	9
32	resyn3	7840	0.1	0.1	0.3	0.2	1952	0	0
32	dc2	7840	0.1	0.1	0.2	0.3	1952	0	0
32	complex	7839	TO	TO	0.2	0.4	1948	0	9
64	resyn	32064	0.3	TO	1.0	5.6	7996	1	10
64	resyn2	32064	0.2	TO	1.0	5.9	7996	1	9
64	resyn3	32064	0.3	0.2	1.0	5.6	8000	0	0
64	dc2	32064	0.2	0.3	1.0	5.8	8000	0	0
64	complex	32063	TO	TO	1.0	6.3	7996	0	9
128	resyn	129664	1.3	TO	5.7	200.6	32380	1	10
128	resyn2	129664	1.2	TO	6.4	214.1	32380	1	9
128	resyn3	129664	1.2	TO	7.7	209.3	32384	0	0
128	dc2	129664	1.1	TO	6.6	214.6	32384	0	0
128	complex	129663	TO	TO	5.8	214.1	32380	0	9

**Table 1.** Results on ABC benchmarks with bit-width  $n$ .

*Benchmarks.* We evaluate our approach on integer multiplier circuits. Multipliers consist of three main components: partial product generation (PPG), partial product accumulation (PPA), and a final-stage adder (FSA). Each component has optimized architectures to reduce space and delay.

Two encodings are frequently used for PPG: simple AND-gate-based generation or Booth encoding. In the former case, every partial product  $a_i b_j$  is explicitly computed, hence we do not require extension variables in our approach. For Booth encoding, we require extension variables as the partial products are internally combined. During PPA, partial products are accumulated, with the final two layers summed in the FSA.

In structured circuits, PPG, PPA, and FSA are clearly defined, benefiting tools like AMULET2 and TELUMA that require a clear cut between PPA and FSA to simplify the FSA. In synthesized circuits, gates are merged and rewritten to optimize the circuit, which blurs these component boundaries, and complicates direct verification. We consider two sets of benchmarks:

- *aoki-multipliers* [13]: This set of benchmarks contains 192 different non-synthesized multiplier architectures with an input bit-width 64.
- *synthesized ABC multipliers* [1]: These multipliers are generated using different types of standard synthesis scripts within ABC: *resyn*, *resyn2*, *resyn3*, *dc2*. We include a *complex* script that combines several synthesis techniques<sup>1</sup>.

### 5.3 Results

The results for the synthesized ABC multipliers are shown in Table 1. The heuristics of AMULET2 and TELUMA are not robust for these benchmarks and

<sup>1</sup> `-c "logic; mfs2 -W 20; ps; mfs; st; ps; dc2 -1; ps; resub -1 -K 16 -N 3 -w 100; ps; logic; mfs2 -W 20; ps; mfs; st; ps; iresyn -1; ps; resyn; ps; resyn2; ps; resyn3; ps; dc2 -1; ps;"`



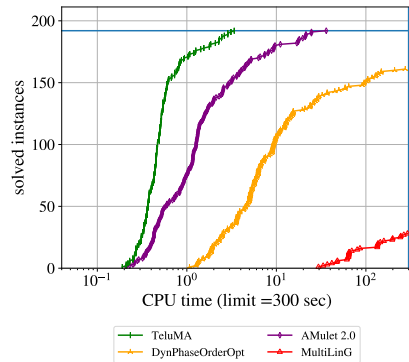


Fig. 2. Results of aoki-benchmarks

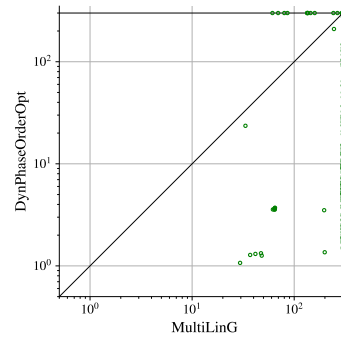


Fig. 3. Comparing MULTI Ling and DYNPhaseOrderOpt

produce time outs. DYNPhaseOrderOpt and our tool MULTI Ling are both able to solve all benchmarks within the time limit of 300 seconds. We provide statistics on MULTI Ling and show how often nodes with equal inputs are merged (“MergedNodes”), the number of eliminated positive nodes (“PosNodes”), and how often a local  $\prec_{\text{drl}}$ -Gröbner basis is computed (“LocalGB”). In none of the benchmarks we detected equivalent nodes. Interestingly for “resyn3” and “dc2” everything could be linearized via merging nodes with equal inputs.

Figure 2 shows the results on the aoki-benchmarks. Both, TELUMA and AMULET2, are able to solve the complete benchmark set. DYNPhaseOrderOpt solves 163 out of 192 benchmarks, whereas our approach is only able to solve 30 benchmarks. Although the number of solved instances is low for MULTI Ling, we are able to solve 14 out of the 29 benchmarks that DYNPhaseOrderOpt does not cover, which is shown in Figure 3. As an example, among those 14 instances is a circuit consisting of a simple PPG, a grid-like PPA, and a carry-lookahead adder as FSA. The circuit has 53861 nodes and it was solved in MULTI Ling by merging nodes with equal inputs 8002 times, removing positive nodes 7811 times and finally computing a local  $\prec_{\text{drl}}$ -Gröbner basis 3999 times. All instances that MULTI Ling could not solve timed out during the Gröbner bases computations.

*Summarizing the evaluation, AMULET2 and TELUMA are highly efficient on the structured circuits but are not robust on synthesized benchmarks. DYNPhaseOrderOpt and MULTI Ling are both robust and complement each other on complex multiplier designs. Hence we believe that our proposed approach is a valuable addition to the algebraic verification landscape and will be even more powerful when it is combined with existing methods.*

## 6 Conclusion

In this paper we have presented a novel technique to verify directed acyclic graphs using computer algebra. Our first contribution is a theoretical theorem that shows how we can perform the ideal membership test of a specification

polynomial using only linear polynomial operations. Secondly, we discuss how we can apply this theorem in practice to overcome the double-exponential complexity of computing a Gröbner basis. We present a technique that incrementally computes Gröbner bases for small sub-graphs to extract the linear information of the polynomials. We have demonstrated the potential of our approach on a set of multiplier circuits that have been challenging to verify so far.

In the future we aim to turn the black-box Gröbner basis approach into a white-box and explore how we can derive the linear polynomials without the computation of a full Gröbner basis. We also envision equivalence checking as a potential application, as this restricts the computation to Boolean polynomials.

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## A Complete Gröbner basis for two-bit multiplier

$gb[1]=110-t00$	$gb[27]=116*a1-116$
$gb[2]=s0-110$	$gb[28]=b0^2-b0$
$gb[3]=112-t10$	$gb[29]=t10*b0-t10$
$gb[4]=114-t01$	$gb[30]=t00*b0-t00$
$gb[5]=118-116+t01+t10-1$	$gb[31]=116*b0-116$
$gb[6]=120+2*116-t01-t10$	$gb[32]=b1^2-b1$
$gb[7]=s1-120$	$gb[33]=t11*b1-t11$
$gb[8]=122-t11$	$gb[34]=t10*b1-t11*b0$
$gb[9]=124-116$	$gb[35]=t01*b1-t01$
$gb[10]=126-124+116+t11-1$	$gb[36]=t00*b1-t01*b0$
$gb[11]=128+2*124-116-t11$	$gb[37]=116*b1-116$
$gb[12]=s2-128$	$gb[38]=t11^2-t11$
$gb[13]=s3-124$	$gb[39]=t10*t11-t11*b0$
$gb[14]=a0^2-a0$	$gb[40]=t01*t11-t11*a0$
$gb[15]=b0*a0-110$	$gb[41]=t00*t11-116$
$gb[16]=b1*a0-t01$	$gb[42]=116*t11-124$
$gb[17]=t01*a0-t01$	$gb[43]=t10^2-t10$
$gb[18]=t00*a0-t00$	$gb[44]=t01*t10-116$
$gb[19]=116*a0-116$	$gb[45]=t00*t10-t10*a0$
$gb[20]=a1^2-a1$	$gb[46]=116*t10-116$
$gb[21]=b0*a1-t10$	$gb[47]=t01^2-t01$
$gb[22]=b1*a1-t11$	$gb[48]=t00*t01-t01*b0$
$gb[23]=t11*a1-t11$	$gb[49]=116*t01+116*t10+120-t01-t10$
$gb[24]=t10*a1-t10$	$gb[50]=t00^2-t00$
$gb[25]=t01*a1-t11*a0$	$gb[51]=116*t00-116$
$gb[26]=t00*a1-t10*a0$	$gb[52]=116^2-116$